

Mark M. Tehranipoor

Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity

Associate Chair for Research and Strategic Initiatives, Fellow of IEEE

Co-director, Florida Institute for Cybersecurity (FICS) Research

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FICS Research: <http://fics.institute.ufl.edu/> , Personal: <http://tehranipoor.ece.ufl.edu/index.html>

Email: tehranipoor@ece.ufl.edu , Gmail: tehranipoormark@gmail.com

Research Interests

Hardware Security and Trust, IoT Security, Supply Chain Security, Counterfeit Electronics Detection and Prevention, Reliable Circuit Design and Analysis, and Integrated Circuits and Systems Testing

Academic Appointments

- 07/16-Present Associate Chair for Research and Strategic Initiatives, ECE Department, University of Florida
- 07/15-Present Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity
- 07/15-Present Founder, Co-director, Florida Institute in Cybersecurity (FICS) Research
<http://fics.institute.ufl.edu/>
- 07/15-Present Professor, University of Florida
- 11/13-07/15 Professor, University of Connecticut
- 11/13-08/14 Charles H. Knapp Associate Professor in Electrical Engineering, University of Connecticut
- 04/12-11/13 F.L. Castleman Associate Professor in Engineering Innovation, University of Connecticut
- 08/10-08/13 Associate Professor, Electrical and Computer Department, University of Connecticut
- 08/06-08/10 Assistant Professor, Electrical and Computer Department, University of Connecticut
- 08/08-08/11 Term member of Graduate Faculty, Duke University
- 08/04-08/06 Assistant Professor, Department of Computer Science and Electrical Engineering (CSEE), University of Maryland Baltimore County (UMBC)

Major Initiatives and Accomplishments

- Aug 2017 Led establishing the Trusted and Assured MicroElectronics (**TAME**) Forum (<http://www.tameforum.org/>). TAME Forum's objective is to provide a bi-annual platform to researchers in academia, and practitioners in industry and government to discuss innovative solutions in the domain of trusted microelectronics in today's globalized and complex supply chain, discuss grand challenges and identify collaboration

opportunities. One major outcome of the TAME Forum is expected to be the first ever “National Technology Roadmap for Trusted and Assured Microelectronics”.

- Aug 2017 New ACR initiative, **Faculty Development Program**: This program is intended to build a strong foundation for the success of our junior faculty (assistant and associate professors). Many new faculty have had little or no exposure to the different and new aspects of their profession, and desire an experienced voice to guide them in tailoring the initial stages of a successful career. Hence, it is critical to continually provide opportunities for career development through a strong voluntary mentor/mentee relationship. As a result, we established flexible career guidance and mentoring program to create a nurturing environment within the ECE department.
- March 2017 Led the **2017 FICS Research Annual Conference on Cybersecurity** (<http://fics-institute.org/outreach/conference/>). More than 210 attended the conference from academia, industry, and government. The event was supported by 13 companies, more than 20 demos and 50 posters were presented, with many companies and government labs active in recruiting students for full time and summer intern positions.
- Jan 2017 Helped establish **CyberGators**, and currently serving as the faculty advisor. CyberGators is a fully student-run organization at the FICS Research Institute. CyberGators group includes four major committees namely Incident Analysis and Reporting, IoT Hacking, Outreach and Diversity, and Professional Development. CyberGators mission is to advance the state of art in cybersecurity and increase students professional development by providing opportunities to communicate with experts from academia, industry, and government.
- Dec. 2016 Worked closely with the lead PI Prof. Bhunia on an **NSF Scholarship for Service (SFS)**. The accepted proposal, in collaboration with FIU, received \$4.6M to recruit BS, MS and PhD students for a new program called *Hardware and Systems Security (HSS)* jointly developed at the UF ECE/CISE and FIU ECE department. The target program will be made available online through UF EDGE program. The EDGE capability will allow FIU students to take the basic HSS classes and then continue with other cybersecurity courses in their respective departments. The program is available nation wide to all students from ECE, CSE, ME, BME, and other departments.
- August 2016 Led establishment of **SCAN Lab under FICS Research Institute**. The lab includes \$10M equipment with capabilities for physical inspection, imaging capabilities, attack assessment, electrical tests and measurement, bio-medical tests, thermal test, device characterization, etc. Prof. Forte is currently serving as the director for SCAN Lab.
- April 2016 The topic of hardware security has seen major growth over the past decade or so. However, the community never enjoyed a dedicated journal on this topic, hence my colleague Prof. Bhunia and I took on this challenge and established the first ever journal supported by Springer called **Journal of Hardware and Systems Security (HASS)**, <http://www.editorialmanager.com/hass>
- April 2016 Helped establish **IEEE Symposium on Asian Hardware-Oriented Security and Trust (HOST)**. AsianHOST Symposium brings together experts from Asia, Europe and North America together to establish collaboration on topics related to Hardware Security. <http://asianhost.org/>
- Feb 2016 **UF-TESCAN Partnership**: Led this effort to establish a partnership with one of the leading electron microscope companies in the world. This partnership is worth about \$5M. The partnership includes significant donation, 5-year warranty, monthly meeting

- with TESCAN to develop strategies for collaboration and joint proposals to government and industry, student training, joint publications, etc. <http://fics.institute.ufl.edu/facilities/>
- Feb 2016 Led the establishment of the **2016 FICS Annual Conference on Cybersecurity**. The goal of this conference was to put together a program consisting of experts from industry, government, and academia to discuss cybersecurity problems, engage with students via poster sessions and evaluation, project demos, panels, competitions, etc. The first year event brought together more than 155 experts on campus. The 2016 conference was sponsored by more than 12 companies. <http://fics.institute.ufl.edu/conference/>
- July 2015 Founded the **Florida Institute for Cybersecurity (FICS) Research** to become a premier institute on cybersecurity that covers device to systems, human, mobile, network, software, to enterprise security. <http://fics.institute.ufl.edu/>. Currently serving as co-director for FICS Research.
- Nov. 2015 **CDC Tool** became part of **SAE international standard, AS6171**. The CDC project was sponsored in part by Honeywell, Comcast, and Missile Defense Agency (MDA). The tool is the first of its kind to evaluate the efficiency of test and inspection techniques for counterfeit and fake chips. *The tool was acquired by SAE International.*
- April 2015 Initiated **Connecticut Cybersecurity Center (C3)** at the University of Connecticut. I led a proposal for a total of \$1M funded for state of Connecticut. The fund allowed for recruiting two new faculty and a full time staff.
- Nov 2014 Helped with the effort to establish a **Center of Excellence in Microscopy** at the University of Connecticut. This is a multi million dollar partnership between UConn and FEI. <http://today.uconn.edu/blog/2014/10/new-collaboration-to-create-world-class-microscopy-center/>
- Oct. 2014 Led establishment of **CyberSEED (Cybersecurity, Education, and Diversity Challenge Week)**. <http://www.csi.uconn.edu/cybersecurity-week>. CyberSEED, supported by more than a dozen companies, brought together students (undergraduate and graduate) from more than 45 schools and colleges around the nation to compete on many cybersecurity problems on campus at UConn. The students competed on capture the flag (CTF), software security, and hardware security.
- May 2014 **Lead PI for MURI grant from DOD AFOSR**. The U.S. Department of Defense awarded a \$7.5 million grant to the University of Connecticut, University of Maryland, and Rice University to support research that will analyze and upgrade security protections for nanoscale computer hardware. UCONN with 6 PIs is the lead institution and University of Maryland (2PIs) and Rice University (1 PI) are the other collaborators. <http://news.engr.uconn.edu/muri-grant-to-improve-the-security-of-nanoscale-computer-devices.php>. **This was the single largest grant brought to the University of Connecticut.**
- 2012-2015 Led establishment of **CHASE Consortium**: Established a consortium by bringing together several companies and agencies including Missile Defense Agency (MDA), Honeywell, Juniper, Comcast, and Semiconductor Research Corporation (SRC), UTAS, etc.
- April 2014 **Founding Director for CSI Center at UConn**: The School of Engineering at the University of Connecticut, in partnership with Comcast inaugurates a signature initiative, establishing **Center of Excellence in Security Innovation (CSI)**. The CSI's mission is to lead research, teaching and workforce development in hardware, software, and network security. CSI was established in April 2014 with main support from Comcast.

- Comcast provided more than 3 years of collaboration and support with CHASE prior to engaging with CHASE on establishing CSI. <http://www.csi.uconn.edu/>
- June 2012 Established the **Center for Hardware Assurance, Security, and Engineering (CHASE)**. The Center was established in 2012 to provide the University of Connecticut with a physical and intellectual environment necessary for interdisciplinary hardware-oriented research and applications to meet the challenges of the future in the field of assurance and security. CHASE is a research consortium with member companies from across the nation committed to enabling knowledge breakthroughs that shape future electronic systems. Current members include Honeywell, Comcast, Missile Defense Agency (MDA), and Juniper Networks. Other sponsors include Synokey, LSI, Qualcomm, Cisco, Samsung, Mangolia, R3Logic, Freescale, SRC, GRC, and more. <https://www.chase.uconn.edu/>
- Feb. 2012 Established the **Workshop on Hardware and Systems Security at UConn**. The workshop grew quite fast that went from 60 participants in 2012 to 220 in 2014. We were able to bring together experts from academia, industry, and government to discuss the challenging problems of hardware and cyber security.
- Feb 2011 Led establishment of **Trust-Hub** (www.trust-hub.org) funded by the National Science Foundation (NSF). Trust-Hub is a website where members of the IC hardware security community can share their discoveries and other information that accelerates hardware security research and developments. Trust-Hub serves as a clearing house and community-building tool where researchers can exchange papers, benchmarks, hardware platforms, source codes and tools.
- Jan 2008 Led the establishment of the IEEE Workshop on **Hardware-Oriented Security and Trust (HOST)**, with Dr. Jim Plusquellic of UNM. In 2010, HOST became a symposium and is now the premier event on hardware security. HOST moved to Washington DC area in 2013 and grew to become an event with more than 350 attendees by 2017. <http://www.hostsymposium.org/>
- 2006-2016 Published the **first series of books on Hardware Security and Trust**. One of the books is currently being used as text book in the domain of hardware security. <http://tehranipoor.ece.ufl.edu/publications.html>

Education

- 1/02 – 8/04 Ph.D, Electrical and Computer Eng., University of Texas at Dallas, Jan 2002-Aug. 2004.
- 9/97 – 8/00 M.Sc. Electrical Engineering, University of Tehran, 1997-2000
- 1/92 – 8/97 B.Sc. Electrical Engineering, Tehran Polytechnic University, 1992-1997

Project Sponsors

1. National Science Foundation (NSF)
2. Semiconductor Research Corporation (SRC)
3. Global Research Corporation (GRC)
4. National Institute of Standards and Technology (NIST)
5. Office of Naval Research (ONR)

6. Army Research Office (ARO)
7. Missile Defense Agency (MDA)
8. GAANN, Department of Education
9. Defense Advanced Research Projects Agency (DARPA)
10. Air Force Office of Scientific Research (AFOSR) – MURI
11. KCP, Department of Energy (DOE)
12. AFOSR / DURIP
13. OSD/ONR SBIR
14. DRAPER
15. Raytheon
16. Tektronix
17. Texas Instruments
18. Cisco
19. Qualcomm
20. LSI Corporation
21. Freescale Semiconductor
22. MediaTek
23. Comcast
24. Honeywell
25. Juniper
26. BRIDG
27. Mentor Graphics
28. Intel
29. R3Logic
30. Synokey
31. UF Office of Research
32. CRI/Rambus Donation
33. Verigy, Inc. Donation
34. Xilinx Donation
35. Agilent Donation
36. EPSRC of United Kingdom
37. UConn Research Foundation
38. UMBC RAS/RIS
39. *Small donations:*
 - IBM

- Intel
- Raytheon
- Draper
- TESCAN
- ZEISS
- Thales E-security
- Texas Instruments
- Rambus
- Mentor Graphics
- NREL
- Hammamatsu
- Microphotonics
- Cisco
- Angstrom Scientific
- Cybraics
- Athena Groups
- Raith
- Bruker
- United Technology Research Center
- Microsemi
- Applied DNA Sciences
- Micronet Solutions
- PFP Technologies

Research Supports and Donations (PI and Co-PI): \$\$\$M

Funding information will be provided upon request.

Industry Experience

1/98 – 11/01 **Advanced DSP Research Center, SAM Communications**

Designing emulator boards for TMS320C54x DSP, Implementing different programs on 'C54x emulator, internal memory BIST and implementation on 'C54x DSP.

In the Press

Vulnerability Note VU#739007

<http://www.kb.cert.org/vuls/id/739007>

Crypto Bugs in IEEE Standard Expose Intellectual Property in Plaintext

<https://www.bleepingcomputer.com/news/security/crypto-bugs-in-ieee-standard-expose-intellectual-property-in-plaintext/>

Flaws in IEEE P1735 electronics standard expose intellectual property

<http://securityaffairs.co/wordpress/65184/hacking/ieee-p1735-electronics-standard-flaws.html>

IEEE Spectrum, M. Tehranipoor, U. Guin, and S. Bhunia, **“Invasion of the Hardware Snatchers: Fake Hardware Could Open the Door to Malicious Malware and Critical Failure,”** IEEE Spectrum, 2017.

<http://spectrum.ieee.org/computing/hardware/invasion-of-the-hardware-snatchers-cloned-electronics-pollute-the-market>

UF’s Annual Cybersecurity Conference Focuses on Security of IoT

<https://www.eng.ufl.edu/newengineer/ece/fics-2017/>

Interview with Le Monde France: Fight against counterfeit electronic components

http://www.lemonde.fr/sciences/article/2016/12/05/lutter-contre-la-contrefacon-de-composants-electroniques_5043610_1650684.html

Pensacola News Journal: Cybersecurity must increase with automation

<http://www.pnj.com/story/money/business/2016/11/28/cybersecurity-must-increase-automation/94546842/>

UF Partners with TESCAN to create world-class hardware security lab

http://www.strategic-directions.com/_a/industry-news/?action=2&terms=&sdi=26f5e7d4-b522-47e8-8c6e-63a1474edbf

University of Florida Cybersecurity Team Turns to Tektronix to Outfit Electronics Security Lab

<http://finance.yahoo.com/news/university-florida-cybersecurity-team-turns-130000458.html>

WUFT, Nov. 15, 2015, Cybersecurity Discussion Raises Concern For Experts

<http://www.wuft.org/news/2015/11/15/cybersecurity-discussion-raises-concern-for-experts/>

IEEE Spectrum

<http://spectrum.ieee.org/tech-talk/telecom/security/an-unhackable-qr-code-to-fight-bogus-chips>

BusinessWire:

NIST Cybersecurity advisor visited CHASE center, Feb. 2014.

http://www.businesswire.com/news/home/20150219005203/en/NIST-Cybersecurity-Chief-Discuss-Threats-Framework-Implementation#.VOX_2MYsO8I

Yahoo Finance:

<http://finance.yahoo.com/news/university-connecticut-comcast-sponsor-first-130000543.html>

Washington Times

<http://www.washingtontimes.com/news/2014/apr/29/universities-to-research-nanotechnology-security/>

Wall Street Journal

<http://online.wsj.com/article/PR-CO-20140410-912537.html>

Universities beef up cybersecurity, identity theft research

<http://gcn.com/blogs/pulse/2014/04/ut-uconn-cybersecurity-research.aspx>

Credit Card Data Theft: Stopping the Hackers

<http://today.uconn.edu/blog/2014/03/credit-card-data-theft-stopping-the-hackers/>

Expert Discusses Steps to Address Threat of Cyber Attacks

<http://today.uconn.edu/blog/2013/10/expert-discusses-steps-to-address-threat-of-cyber-attacks/>

Cover Story, IEEE Spectrum, The Hidden Dangers of Chop-Shop Electronics

<http://spectrum.ieee.org/semiconductors/processors/the-hidden-dangers-of-chopshop-electronics>

Conference on Counterfeit Electronics Addresses Growing National Concern

<http://www.chase.uconn.edu/conference-on-counterfeit-electronics-addresses-growing-national-concern.php>

Sen. Lieberman Praises UConn Cybersecurity Labs

<http://today.uconn.edu/blog/2012/02/sen-lieberman-praises-uconn-cybersecurity-labs/>

Lieberman pushes for cyber security

<http://www.dailycampus.com/news/lieberman-pushes-for-cyber-security-1.2794957#.T1P6RvEgdGM>

Research Initiative Will Enhance Integrity of Integrated Circuits

<http://today.uconn.edu/?p=34063>

University of Connecticut and Duke University Develop Unique Method to Improve Testing for Small Delay Defects in Semiconductors

<http://www.hartfordbusiness.com/news14048.html>

<http://www.physorg.com/news199362652.html>

http://www.advn.com/news_University-of-Connecticut-and-Duke-University-Develop-Unique-Method-to-Improve-T_43665962.html

<http://www.forbes.com/feeds/businesswire/2010/07/20/businesswire142648135.html>

<http://www.src.org/newsroom/press-release/2010/86/>

NYU-Poly and UConn Researchers Develop New Design Techniques to Protect Against Vulnerabilities in the Electronics Supply Chain

<http://www.marketwatch.com/story/student-hackers-and-a-dose-of-skepticism-secure-vital-hardware-2011-11-08>

Xuehui Zhang Received First Place Prize at the 2010 CSAW - Embedded Systems Challenge

http://www.brooklyneagle.com/categories/category.php?category_id=31&id=39204

<http://www.poly.edu/press-release/2010/11/02/who-will-protect-our-digital-future-woman-high-school-videographer-student->

Interview with “The Economist”

Interview with EBN

Interview with NPR (twice)

Interview with WUFT

Awards & Honors

- 2017 **IEEE Fellow**
- 2017 **Outstanding Paper Award**, E. L. Principe, N. Asadizanjani, D. Forte, M. Tehranipoor, R. Chivas, M. DiBattista, S. Silverman, M. Marsh, J. Mastovich, J. Odum, “**Steps Towards Automated Deprocessing of Integrated Circuits**,” International Symposium on Test and Failure Analysis (ISTFA), 2017
- 2017 **College of Engineering Excellence in Leadership Award**, University of Florida
- 2017 **ECE Research Excellence Award**, ECE Department, University of Florida
- 2017 **Best Paper Award**, X. Wang, Y. Guo, T. Rahman, D. Zhang, and M. Tehranipoor, “**DOST: Dynamically Obfuscated Wrapper for Split Test against IC Piracy**,” IEEE Asian Hardware-Oriented Security and Trust Symposium (**AsianHOST**), 2017.

- 2017 The article "**Hardware Trojans: Lessons Learned After One Decade of Research**" published in IEEE Transactions On Design Automation of Electronic Systems (TODAES) was included the **21st Annual Best of Computing** (<http://www.computingreviews.com/recommend/bestof/notableitems.cfm?bestYear=2016>).
- 2016 **TTTC Most Successful Event Award for HOST Symposium, Co-founded by Tehranipoor**
- 2016 **Best Paper Award**, Q. Shi, N. Asadi, D. Forte, and M. Tehranipoor, "**A Layout-driven Framework to Assess Vulnerability of ICs to Microprobing Attacks**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016.
- 2016 **Best Paper Candidate**, K. Yang, D. Forte, and M. Tehranipoor, "**UCR: An Unclonable Chipless RFID Tag**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016.
- 2015 **Best Paper Award**, "K. Xiao, D. Forte, and M. Tehranipoor, "**Efficient and Secure Split Manufacturing via Obfuscated Built-In Self-Authentication**," IEEE Hardware-Oriented Security and Trust (HOST), 2015"
- 2015 The paper titled "**Counterfeit Integrated Circuits: Detection, Avoidance, and the Challenges Ahead**" was recognized by JETTA as the most downloaded article in 2014
- 2015-present Intel Charles E. Young Preeminence Endowed Professor in Cybersecurity, University of Florida
- 2015-present Elected member of Connecticut Academy and Science and Engineering (CASE)
- Nov. 2014 ISE North America, US and Canada, **Best Project finalist** for establishing CHASE and CSI centers
- Nov. 2014 **Best paper Candidate**, International Symposium on Test and Failure Analysis (ISTFA), 2014
- Oct. 2014 ISE Northeast, **Best Project finalist** for establishing CHASE and CSI centers
- Aug 2014 Air Force Office of Scientific Research (AFOR) MURI Award (2014-2019)
- Sep. 2014 UConn **ECE Research Excellence** Award
- 2012- 2014 Charles Knapp Associate Professor
- May 2013 **Best Paper Award**, IEEE North Atlantic Test Workshop (NATW), 2013
- 2012 IEEE Computer Society **Golden Core Inductee**
- Oct. 2012 **Best Student Paper Award**, IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), 2012
- 2011- 2012 F.L. Castleman Associate Professor in Engineering Innovation
- June 2012 IEEE Computer Society Outstanding Contribution Award
- April 2012 SOE Outstanding Faculty Advisor Award
- Jan 2012 **Best Special Session Award, IEEE VLSI Test Symposium (VTS), 2011**
- 2010-2013 **IEEE Computer Society Distinguished Speaker**
- 2010-2013 **ACM Distinguished Speaker**
- May 2010 Recipient of the IEEE Computer Society TTTC **Most Successful Technical Event** for founding HOST Symposium

May 2010 Recipient of the 2009 **IEEE Computer Society Certificate of Appreciation**

May 2009 UConn **ECE Research Excellence Award**, 2009

Jan. 2009 **NSF CAREER Award**, 2009

May 2009 **Best Paper Award**, IEEE North Atlantic Test Workshop, 2009

Oct. 2008 **IEEE Computer Society Meritorious Service Award**, 2008

May 2008 **Best Paper Award**, IEEE North Atlantic Test Workshop, 2008

May 2008 Honorable Mention for **Best Paper Award**, IEEE North Atlantic Test Workshop, 2008

May 2007 **Best Panel Award**, IEEE VLSI Test Symposium (VTS), 2006

Nov. 2006 **Top Ten Recognition Paper**, ITC 2005

March 2006 **Best Paper Award**, IEEE VLSI Test Symposium (VTS), 2005

April 2006 **Best Paper Candidate**, Design Automation Conference, 2006

Sep. 2005 **Best Paper Candidate**, TI Symposium on Test (TIST), 2005

1/02 – 08/04 Received Texas Public Educational Grant, 2002-2004

July 1997 **Ranked 2nd**, Undergraduate Program, ECE Department, Tehran Polytechnic University

June 1992 **Ranked 1st**, High School, Among all high school students in Golestan province, Iran

Students Awards from their Projects under my Supervision

- **Best Poster Award supported by DRAPER**, Andrew Stern, Haoting Shen, Xiaolin Xu, Domenic Forte, Mark Tehranipoor, **Near Field EM for Foundry of Origin Identification**, 2017 FICS Annual Conference on Cybersecurity
- **Best Poster Award**, Gustavo K. Contreras, Adib Nahiyani, Domenic Forte, Mark Tehranipoor, **Track and Extract: Information Flow Tracking for Security Vulnerability Analysis and Exploit Extraction**, 2017 FICS Annual Conference on Cybersecurity
- **Best Poster Award**, Troy Bryant, Sreeja Chowdhury, Domenic Forte, Mark Tehranipoor, Nima Maghari, **An All Digital PUF (Physically Unclonable Functions) for AMS Applications Using Stochastic Comparator Voltage Offset**, 2017 FICS Annual Conference on Cybersecurity
- Adib Nahiyani and Gus Contreras receive **Best Poster Award** at the 2016 FICS Annual Conference on Cybersecurity, Title: **DSeRC: Design Security Rule Check**
- Mehdi Sadi received **Best in Session Award** from TECHCON, 2016 for his paper titled **BIST-Assisted In-field Aging Reliability Management of SoCs Using On-Chip Clock Sweeping and Machine Learning**
- G. Contreras received **Best in Session Award** from TECHCON, 2016 for his paper titled **Fault Deterministic Vector Analysis and Seed Extraction for LBIST**
- Tauhid Rahman received **Best in Session Award** from TECHCON, 2016 for his paper titled **SRAM Inspired Design and Optimization for Developing Robust Security Primitives**
- **Qihang Shi** received the Best TA Award from the ECE Department, UConn, 2012
- **Andrew Ferraiuolo, Adam Zimmer, and Rifat Chowdhury** won the first prize from ECE on their Senior Design Project under my supervision, 2012

- **Nicholas Tuzzio, Xuehui Zhang and Andrew Ferraiuolo:** Received the first place prize at the 2011 CSAW - Embedded Systems Challenge (Physical Unclonable Functions)
- **Xuehui Zhang, Nicholas Tuzzio, and Andrew Ferraiuolo:** Received the third place prize at the 2011 CSAW - Embedded Systems Challenge (Malicious Processor Design)
- **Junxia Ma:** Selected as one of the four finalists for Connecticut Women of Innovation (WOI)
- **Brian Helfer, Theodore Estwan, and Emilio Cepeda** won the first prize from ECE on their Senior Design Project under my supervision, 2011
- **Xuehui Zhang:** Received First Place Prize at the 2010 CSAW - Embedded Systems Challenge
- **Michel Wang:** Received Best in Session Award at TECHCON 2010
- **Nisar Ahmed:** Received UConn SOE Outstanding Graduate Thesis Award
- **Joseph Larosa, Corey Benoit, Andrew Tan, and Kevin Perkins** won the first prize from ECE on their Senior Design Project under my supervision, 2010
- **Junxia Ma:** Received Best in Session Award at TECHCON 2009
- **Jeremy Lee:** Received the TTTC Best Thesis Research Poster Award, 2008
- **Jeremy Lee:** Received the Best Computer Engineering Seminar Presentation, 2008
- **Paul Rago and Aaron Feldstein** won the second prize from ECE on their Senior Design Project under my supervision, 2008
- **Nisar Ahmed:** Received the TTTC 2007 Best Doctoral Dissertation Award
- **Kevin Tyler, Danny Ho, and Vimal Vachhani** won the first prize from ECE on their Senior Design Project under my supervision, 2007
- **Nisar Ahmed:** Received the UMBC-CSEE's Best PhD Thesis Award, 2006

Professional Activities

Founding Positions:

- **Co-Organizer**, Physical Attacks and Inspection on Electronics (**PAINE**), co-located with DAC 2018
<http://paine-workshop.org/>
- **Founder**, Trusted and Assured Microelectronics Forum (**TAME**)
www.tameforum.org
- **Co-founder**, Journal of Hardware and Systems Security (**HASS**), 2016
<http://www.editorialmanager.com/hass>
- **Co-founder**, IEEE Asian Symposium on Hardware-Oriented Security and Trust (**AsianHOST**), 2016
<http://asianhost.org/index.htm>
- **Co-Founder**, International Verification and Security Workshop (**IVSW**) and member of the steering committee,
<http://tima.imag.fr/conferences/ivsw/ivsw16/>

- **Founder**, Co-director, Florida Institute for Cybersecurity (**FICS**), 2015-present
<http://www.institute.ufl.edu>
- **Founding Director**, Center for Hardware Assurance, Security, and Engineering (**CHASE**), 2012-2015 <http://www.chase.uconn.edu/>
- **Founding Director**, Comcast Center of Excellence in Security Innovation (**CSI**), 2013-2015
<http://www.csi.uconn.edu/>
- **Co-founder**, IEEE Int. Symposium on Hardware-Oriented Security and Trust (**HOST**), 2008
<http://www.engr.uconn.edu/HOST/>
- **Co-founder**, Trust-Hub, 2010
<http://www.trust-hub.org/>

IEEE/ACM Events Chair Positions:

- **Editor-in-Chief**, Journal of Hardware and Systems Security (HASS), 2016-present
- 2018 IEEE CS **Fellows Evaluation Committee**
- **IEEE Cybersecurity Initiative Ambassador** (2016-present)
- **Co-Program Chair**, International Verification and Security Workshop (IVSW), 2016
- **Co-Program Chair**, IoT and Automotive Security Workshop (ISAW), 2017
- **Co-program Chair**, IEEE International Workshop on Cross-Layer Cyber-Physical Systems Security (CPSS), 2016
- **Co-program Chair**, IoT Security Workshop, co-located with IEEE HOST 2017
- **Associate EIC**, IEEE Design & Test of Computers, 2012-2014
- **Vice-General Chair**, IEEE North Atlantic Test Workshop (NATW), 2011
- **General Chair**, IEEE Workshop on Defect and Data Driven Testing (D3T), 2009, Austin, TX
- **General Chair**, IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems (DFT), 2009, Chicago, IL
- **General Chair**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2009, San Francisco, CA
- **General Chair**, 1st IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2008, Anaheim, CA
- **Steering Committee Chair**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2008-present
- **Program Chair**, IEEE Workshop on Defect Based Testing (DBT), 2008, Santa Clara, CA
- **Program Chair**, IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems (DFT), 2008, Boston, MA
- **Program Chair**, IEEE Workshop on Defect Based Testing (DBT), 2007, Santa Clara, CA
- **Local Arrangement Chair**, IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems (DFT), 2006, Washington DC

- **Member, Steering Committee**, IEEE Workshop on Defect and Data Driven Testing (D3T), 2009-2010
- **Member, Steering Committee**, IEEE Workshop on Defect and Adaptive Test Analysis (DATA), 2011-present
- **Member, Steering Committee**, IEEE International Verification and Security Workshop (IVSW), 2016-present
- **Vice-Chair**, TTTC Technical Activity group on Hardware Security and Trust
- **Vice-General Chair**, IEEE North Atlantic Test Workshop (NATW), 2012
- **Co-program Chair**, Internet of Things (IoT) and Automotive Security Workshop (IASW), co-located with HOST Symposium, 2017-present
- **Industry Liaison**, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2014-present
- **Industry Liaison**, Workshop for Women in Hardware and Systems Security (WISE), 2017-present
- **Industry Liaison**, IEEE Asian Symposium on Hardware-Oriented Security and Trust (AsianHOST), 2016
- **Panel Chair**, IEEE Asian Symposium on Hardware-Oriented Security and Trust (AsianHOST), 2016-present
- **Security Special Session Track Chair**, IEEE International Microprocessor Test and Verification (MTV) conference, 2016
- **Security Track Co-chair**, International Test Conference (ITC), 2016-present
- **Security Track Co-chair**, Design Automation Conference (DAC), 2017-present
- **Steering Committee**, Attacks and Solutions in Hardware Security (ASHES), Co-located with CCS 2017

Non-IEEE Events Chair Positions:

- **Co-Chair**, Trusted and Assured Microelectronics (TAME) Forum, Nov. 2017
- **Steering Committee**, Trusted and Assured Microelectronics (TAME) Forum
- **Chair**, FICS Annual Conference on Cybersecurity, March 2017. **13 companies sponsored this event. 210 attended.**
- **Chair**, FICS Annual Conference on Cybersecurity, February 2016. **12 companies sponsored this event. 155 attended.**
- **Chair**, CHASE Conference on Secure/Trustworthy Systems and Supply Chain Assurance, 2015. **10 companies sponsored this event.**
- **Co-organizer**, CyberSEED (<http://www.csi.uconn.edu/cybersecurity-week>), **More than a dozen companies sponsored this event.**
- **Chair**, CHASE Workshop on Secure/Trustworthy Systems and Supply Chain Assurance, 2014 (<https://www.chase.uconn.edu/chase-workshop-2014.php>). **8 companies sponsored this event.**
- **Chair**, ARO/CHASE Sponsored Workshop on Counterfeit Electronics, 2013
- **Chair**, 2nd ARO Sponsored Workshop on Hardware Assurance, 2011

- **Chair**, 1st ARO Workshop on Hardware Assurance, 2009

Editorial Board:

- **Associate Editor**, IEEE Transactions on VLSI (**TVLSI**), 2015-present
- **Associate Editor**, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), 2013-present
- **Associate Editor**, IEEE Design & Test of Computer Magazine, 2009-2015
- **Associate Editor**, Journal of Low Power Electronics (**JOLPE**), 2009-present
- **Associate Editor**, Journal of Electronic Testing: Theory and Applications (**JETTA**), 2007-present
- **Editor**, Test Technology Technical Council (**TTTC**) Newsletter, 2008-2011

Guest Editor:

- C. Chang, M. van Dijk, U. Ruhrmair, and M. Tehranipoor, Emerging Attacks and Solutions for Secure Hardware in the Internet of Things, IEEE Transactions on Dependable and Secure Computing (TDSC)
- IEEE Transactions on Multi-Scale Computing Systems, Special Issue on Hardware/Software Cross-Layer Technologies for Trustworthy and Secure Computing, Shiyun Hu (Michigan Technological University), Yier Jin (University of Central Florida), Mark M. Tehranipoor (University of Connecticut), Kenneth Heffner (Honeywell)
- IET Computers and Digital Techniques, Special Issue on Hardware Security, Ilia Polian (U of Passau) and M. Tehranipoor (UCONN), 2013-2014
- Special issue on "On-chip Structures for Smarter Silicon", IEEE Design & Test of Computers, Co-guest Editor: LeRoy Winemberg (Freescale Semiconductor), 2012
- IEEE Computer Society (CS) Computing Now on Hardware Security and Trust, September 2010
- IEEE Design & Test Special Issue on "Verifying Physical Trustworthiness of Integrated Circuits and Systems", Co-guest Editor: Farinaz Koushanfar (Rice University), 2009
- Special issue on "Test, Defect Tolerance, and Reliability of Nanoscale Devices", Journal of Electronic Testing: Theory and Applications (JETTA), 2007
- Special issue on "IR-Drop and power Supply Noise Effects on Design and Test of Very Deep Submicron Designs", IEEE Design & Test of Computers, Co-guest Editor: Ken Butler (Texas Instruments), 2008

Tutorials

- IEEE International Hardware-Oriented Security and Trust (HOST), **Protecting Electronics Supply Chain from Throughout Lifecycle**, Washington DC, 2018
- IEEE International Hardware-Oriented Security and Trust (HOST), **Protecting Electronics Supply Chain from Design to Resign**, Washington DC, 2017

- International Test Conference (ITC), **Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits**, Dallas/Fort Worth, TX, 2016
- **Dagstuhl Seminar on Hardware Security**, Germany, Dagstuhl, 2016, Title: Hardware Security (<http://www.dagstuhl.de/de/programm/kalender/semhp/?semnr=16202>)
- International Test Conference (ITC), **Test Opportunities and Challenges for Secure Hardware and Verifying Trust in Integrated Circuits**, 2015
- Design Automation Conference (DAC), **Introduction to Hardware Security**, M. Potkonjak (UCLA), M. Tehranipour (UConn), 2015
- IEEE International System-on-Chip Conference (SOCC), **Electronic Component Supply Chain Security: Threats, Challenges, and Solution**, M. Tehranipour (UConn), 2014
- Design, Automation, and Test in Europe (DATE), **All You Need to Know About Hardware Trojans and Counterfeit ICs**, M. Tehranipour and D. Forte (UConn), 2014
- IEEE Conference on VLSI, 2014, **All You Need to Know About Hardware Trojans and Counterfeit ICs**, M. Tehranipour and D. Forte (UConn)
- IEEE International Reliability Physics Symposium (IRPS), 2013, **Chip to System Reliability Fundamentals**, M. Tehranipour (UConn), Nemat Bidokhti (Cisco), and Bill Eklow (Cisco)
- International Test Conference (ITC), 2011, **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**, Srivaths Ravi (Texas Instruments), M. Tehranipour (UConn), and Rohit Kapur (Synopsys)
- International Test Conference (ITC), 2011, **High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges & Solutions**, M. Tehranipour (UConn), Krish Chakrabarty (Duke University), and Jeff Rearick (AMD)
- Design Automation Conference (DAC), 2011, **Chip to System Reliability Fundamentals**, M. Tehranipour (UConn), Nemat Bidokhti (Cisco), and Bill Eklow (Cisco)
- International Test Conference (ITC), 2010, **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**, Srivaths Ravi (Texas Instruments), M. Tehranipour (UConn), and Rohit Kapur (Synopsys)
- International Test Conference (ITC), 2010, **High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges & Solutions**, M. Tehranipour (UConn), Krish Chakrabarty (Duke University), and Jeff Rearick (AMD)
- Design, Automation, and Test in Europe (DATE), 2010, **Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**, Srivaths Ravi (Texas Instruments), M. Tehranipour (UConn), Rohit Kapur (Synopsys)
- International Conference on VLSI Design, Title: **High-Quality and Low-Cost Delay Test for VDSM Designs**, January 2009
- **IEEE MidWest Symposium on Circuits And Systems**, Title: High-Quality Delay Tests for Nanometer Technology Designs, August 2008

Panelist

- Panelist, Global Electronic Supply Chain: What Can South East Asian do about it? IEEE AsianHOST, 2017

- Panelist: Internet of Things (IoT) and Automotive Security Workshop (IASW), 2017
- Panelist: NYU Alfred P. Sloan Foundation, Cybersecurity Lecture, with Wally Rhines, Chairman and CEO of Mentor Graphics, April 2017
- Panelist: International Workshop on Hardware Security, 2016, Title: Research Collaboration Opportunities in Hardware Security Areas
- Panelist: IEEE VLSI Test Symposium (VTS), 2016, Title: Test Challenges for Secure Hardware
- Panelist: International Symposium on Quality Electronic Design (ISQED), 2016, Title: Hardware and Systems Security Challenges in IoT Era
- Panelist: FIU Cybersecurity Conference, October, 2015
- Panelist: IEEE VLSI Test Symposium (VTS), 2015
- Panelist: IEEE S&P Symposium, San Jose, CA, May 2014
- Panelist: SRC STARSS, San Jose, CA, May 2014
- Panelist: Microprocessor Test and verification (MTV), Nov. 2013
- Panelist: IEEE North Atlantic Test Workshop (NATW), May 2013
- Panelist: Cisco innovation Test Conference (CITC), 2012
- Panelist: International Workshop on Defect and Adaptive Test Analysis (DATA), September 2011
- Panelist: International Test Conference (ITC), November 2010
- Panelist: IEEE Symposium on Hardware-Oriented Security and Trust (HOST), June 2010
- Panelist: International Test Conference (ITC), Nov. 2009
- Panelist: International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), October 2009
- Panelist: IEEE Workshop on RTL Testing (WRTL-08), Nov. 2008, Title: Power-Aware Testing in Integrated Circuits

Special Session Organizer:

- **Special Session**, Emerging Topics in Security and Trust I, International Test Conference (ITC), 2017 (Speakers: Brian Dupaix (AFRL), Patrick Schaumont (Virginia Tech), and An Chen (Semiconductor Research Corporation))
- **Special Session**, Emerging Topics in Security and Trust II, International Test Conference (ITC), 2017 (Domenic Forte (University of Florida), Jeyavijayan Rajendran (Texas A&M University), and Krishnendu Chakrabarty (Duke University))
- **Special Session**, Physical Attacks: Can Test Save Us? IEEE VLSI Test Symposium (VTS), 2017, Co-organized by Swarup Bhunia, University of Florida
- **Special Session 1**, IP Protection, IEEE Microprocessor Test and Verification, 2016
- **Special Session 2**, Test for Security and Trust, IEEE Microprocessor Test and Verification (MTV), 2016

- **Special Session**, Test for Security and Trust of Integrated Circuits, International Test Conference (ITC), 2016
- **Special Session**, IEEE VLSI Test Symposium (VTS), 2016, Title: Security Validation in IOT Space
- **Special Session**, IEEE VLSI Design, India, 2016, Title: New Topics in Hardware Security
- **Special Session**, IEEE Microprocessor Test and Verification Workshop (MTV), Austin, 2015, Title: New Directions in Hardware Security
- **HOT Topic Session on Counterfeit Electronics**, IEEE VLSI Test Symposium (VTS), May 2013 (with Prof. Ilia Polian, University of Passau)
- **HOT Topic Session on Smart Silicon**, IEEE VLSI Test Symposium (VTS), May 2011 (with LeRoy Windemberg, Freescale Semiconductor)
- **Moderator, Roundtable on Hardware Security and Trust**, IEEE Design & Test Magazine, September/October 2011

Panel Organizer/Moderator:

- **Panel Organizer**, AsianHOST, Co-organized by Dr. Yousef Iskander, Technical Lead, Cisco
- **Panel Organizer**, Automotive Safety and Security: The Impending Challenges and Hopes on the Horizon, International Test Conference (ITC), 2017, Co-organized by Yervant Zorian, Vice President, Synopsys
- **Panel Organizer**, Test and Security for IoTs, International Test Conference (ITC), 2016
- **Panel Organizer**, IEEE International Verification and Security Workshop (IVSW), 2016, DFT vs. Security – Is it a Contradiction? How Can we Get the Best of Both World?
- **Panel Organizer and Moderator**, IEEE International Hardware-Oriented Security and Trust (HOST), 2016, IP Protection from Chip-to-System Using Reverse Engineering
- **Panel Organizer**, IEEE International Hardware-Oriented Security and Trust (HOST), 2016, Hardware-based System Security
- **Panel Organizer**, IEEE VLSI Test Symposium (VTS), 2016, Test Opportunities for Secure Hardware
- **Panel Organizer**, Design Automation Conference (DAC), 2013 (**Panel 1**: Advanced Node Reliability: Are we in Trouble?)
- **Panel Organizer**, Design Automation Conference (DAC), 2013 (**Panel 2**: Is Security the New Design Dimension?)
- **Panel Organizer/Moderator**, IEEE Hardware-Oriented Security and Trust (HOST), June 2012
- **Moderator**, Special Session on Smart Silicon, IEEE VLSI Test Symposium (VTS), May 2011
- **Panel Moderator**, Title: *Low Power Testing*, IEEE VLSI Test Symposium (VTS), May 2011
- **Panel Organizer**, Title: *Test and Diagnosis for Parametric Failures*, Int. Workshop on Defect and Data Driven Testing, (**D3T**), Nov. 2009
- **Panel Organizer**, Title: *Challenges in Test Data Collection and Analysis*, Int. Workshop on Defect and Data Driven Testing, (**D3T**), Oct. 2008

- **Panel Organizer**, Title: *Zero Defect (Zero DPPM): How can we get there?*, Int. Symposium on Defect and Fault Tolerance in VLSI Systems (**DFT**), Oct. 2008
- **Panel Organizer** (with Kee Sup Kim from Intel), Title: *Three Questions to Oracle (Data required for test engineers and researchers in academia)*, IEEE VLSI Test Symposium (**VTS**), 2006
- **Panel Organizer** (with Hank Walker, Texas A&M University), Title: *Process Variations + Systematic Defects: Can DBT Help?*, International Workshop on Defect-Based Testing (**DBT**), 2007.

Proposal Reviewer/Panelist:

- **National Science Foundation (NSF)**
- **Army Research Office (ARO)**
- **Hong Kong Foundation**
- **Sultanate Oman, Dean of Research**

Membership:

- Fellow, IEEE
- Golden Core Member, IEEE Computer Society
- Member, ACM
- Member, ACM SIGDA
- Member, TTTC
- Member, TTTC Middle East and Africa Group

Program Committee Membership:

- International Symposium on Research in Attacks, Intrusions and Defenses (RAID), 2017
- Microprocessor Test and Verification Workshop, 2012-present
- Smart City Security and Privacy (SCSP), 2016
- ASP-DAC, 2016
- IEEE International Symposium on Computer Architecture and Digital Design (CADS), 2015
- IEEE Int. Symposium on VLSI Design and Test (VDAT), 2014-2015
- EDAA Outstanding Dissertation, European Design and Automation Association (EDAA), 2014-2015
- IEEE Latin American Test Workshop (LATW), 2015
- USENIX, 2014
- CSI International Symposium on Computer Architecture & Digital Systems (CADS 2017)
- Design Automation Conference (DAC), 2011-2014, 2017
- International Symposium on Quality Electronic Design (ISQED), 2014

- TRUDEVICE Workshop on Test and Fault Tolerance for Secure Devices, 2014
- Design Automation Conference (DAC) Panel Committee, 2013
- IEEE Conference on Very Large Scale Integration (VLSI-SoC), 2012-present
- IEEE CS Annual Symposium on VLSI (ISVLSI), 2012-present
- International Test Conference (ITC)-Asia, 2017-present
- International Test Conference (ITC), 2011-present
- Design, Automation, and Test in Europe (DATE), 2009-2010, 2013, 2016-present
- European Test Symposium (ETS), 2010-present
- IEEE VLSI Test Symposium (VTS), 2009-present
- ACM SIGDA PhD DAC Forum, 2008-2011, 2015
- IEEE Workshop on RTL and High Level Testing (WRTLTL), 2009-2011
- ACM Great Lake Symposium on VLSI (GLSVLSI), 2008-present
- International Conference on Communication Theory, Reliability, and Quality of Service (CTRQ), 2008-2013
- IEEE Int. Workshop on Defect Based Testing (DBT), 2005-2010
- Int. Conference on Computer Design (ICCD), 2008-present
- North Atlantic Test Workshop (NATW) 2004-present
- IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), 2005-present
- International Design and Test Workshop (IDT), 2006-present
- International Symposium on Nanoscale Architectures (NanoArch), 2007-2010
- IEEE Int. On-Line Testing Symposium (IOLTS), 2009
- Int. Workshop on Impact of Low-Power Design on Test and Reliability, 2009-present
- Workshop on Unique Chips and Systems (UCAS), 2009
- IEEE Workshop on Design for Reliability and Variability (DRV), 2009

Session Chair:

- International Test Conference (ITC), 2015
- Design Automation Conference, 2015
- DMSMS, 2013
- International Test Conference (ITC), 2013
- Design Automation Conference (DAC), 2012
- Int. Workshop on Current and Defect-Based Testing (DBT), 2005
- Int. Workshop on Current and Defect-Based Testing (DBT'), 2005
- IEEE North Atlantic Test Workshop (NATW), 2006, 2007, 2008, 2009

- International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), 2006
- Design Automation Conference (DAC), 2007
- International Symposium on Nanoscale Architectures (NanoArch), 2008
- International Test Conference (ITC), 2006, 2008, 2009
- IEEE Workshop on RTL and High Level Testing (WRTLTL), 2008
- IEEE VLSI Test Symposium (VTS), 2010
- International Test Conference (ITC), 2013

Session Coordinator:

- International Test Conference (ITC), 2011

External Committee Membership:

- NDIA Systems Security Engineering Committee

Additional Programs

- Robust Design Program (<http://www.robust-designs.com/>)

Review Activity

- National Science Foundation (NSF)
- Army Research Office (ARO)
- Oman, Sultan Ghaboos University Foundation, Dean of Research
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers
- ACM Journal on Emerging Technologies in Computing Systems (JETC)
- ACM Transactions on Design Automation of Electronic Devices (TODAES)
- International Journal of Computers and Applications
- IEEE Circuits, Devices & Systems
- IEEE Design & Test of Computers Magazine
- Journal of Low Power Electronics (JOLPE)
- IBM Journal of Research and Developments
- IEEE Communication Magazine
- IEEE International Test Conference (ITC)

- IEEE VLSI Test Symposium (VTS)
- IEEE Asian Test Symposium (ATS)
- IEEE North Atlantic Test Workshop (NATW)
- IEEE Workshop on Defect-Based Testing (DBT)
- IEEE International Conference on Microelectronics (ICM)
- Design Automation Conference (DAC)
- IEEE Symp. on Defect and Fault Tolerance in VLSI Systems (DFT)
- Great Lake Symposium on VLSI (GLS-VLSI)

Publications

Books

1. Swarup Bhunia and Mark M. Tehranipoor, “**Hardware Security: A Hands-on Learning Approach**”, Elsevier, Morgan Kaufmann imprint, 2018. [Upcoming]
2. M. Tehranipoor, D. Forte, G. Rose, and S. Bhunia, **Security Opportunities in Nano Devices and Emerging Technologies**, CRC Press, 2017.
3. S. Bhunia and M. Tehranipoor, **The Hardware Trojan War: Attacks, Myths, and Defenses**, Springer, 2017.
4. P. Mishra, S. Bhunia, and M. Tehranipoor, **Hardware IP Security and Trust: Validation and Test**, Springer, 2017.
5. D. Forte, S. Bhunia, and M. Tehranipoor, **Hardware Protection through Obfuscation**, Springer, 2017.
6. M. Tehranipoor, U. Guin, and D. Forte, **Counterfeit Integrated Circuits: Detection and Avoidance**, Springer, Dec. 2014
7. M. Tehranipoor, H. Salmani, and X. Zhang, **IC Authentication: Hardware Trojan and Counterfeit Detection**, Springer, Jan. 2014.
8. M. Tehranipoor and C. Wang, **Introduction to Hardware Security and Trust**, Springer, June 2011.
9. M. Tehranipoor, K. Peng, and K. Chakrabarty, **High-Quality Test and Diagnosis for Small Delay Defects**, Springer, July 2011.
10. M. Tehranipoor, **Emerging Nanotechnologies: Test, Defect Tolerance, and Reliability**, Springer, Dec., 2007.
11. M. Tehranipoor and N. Ahmed, **Nanometer Technology Designs: High-Quality Delay Tests**, Springer, Nov. 2007.

Book Chapters

1. Q. Shi, D. Forte, and M. Tehranipoor, “**Deterrent Approaches Against Hardware Trojan Insertion,**” in *Hardware Trojan War*, Springer 2017.

2. S. Bhunia, A. Prasad Deb Nath, and M. Tehranipoor, "**Introduction to Hardware Trojans**," in *Hardware Trojan War*, Springer 2017.
3. F. Rahman, A. Prasad Deb Nath, D. Forte, S. Bhunia, and M. Tehranipoor, "**Nano CMOS Logic-Based Security Primitive**," in *Security Opportunities in Nano Devices and Emerging Technologies*, CRC Press, 2017.
4. H. Shen, F. Rahman, M. Tehranipoor, and D. Forte, "**Carbon-Based Novel Devices for Hardware Security**," in *Security Opportunities in Nano Devices and Emerging Technologies*, CRC Press, 2017.
5. F. Rahman, A. Prasad Deb Nath, S. Bhunia, D. Forte, and M. Tehranipoor, "**Composition of Physical Unclonable Functions: From Device to Architecture**," in *Security Opportunities in Nano Devices and Emerging Technologies*, CRC Press, 2017.
6. B. Shakya, X. Xu, N. Asadi, M. Tehranipoor, and D. Forte, "**Leveraging Circuit Edit for Low-Volume Trusted Nanometer Fabrication**," in *Security Opportunities in Nano Devices and Emerging Technologies*, CRC Press, 2017.
7. U. Guin and M. Tehranipoor, **Obfuscation and Encryption for Securing Semiconductor Supply Chain** in *Hardware Protection through Obfuscation*, 2017.
8. Q. Shi, K. Xiao, D. Forte, and M. Tehranipoor, **Obfuscated Built-in Self Authentication** in *Hardware Protection through Obfuscation*, 2017.
9. T. Rahman, D. Forte, M. Tehranipoor, **Protection of Assets from Scan Chain Vulnerabilities through Obfuscation** in *Hardware Protection through Obfuscation*, 2017.
10. Z. Guo, M. Tehranipoor, and F. Forte, **Permutation based Obfuscation** in *Hardware Protection through Obfuscation*, 2017.
11. B. Shakya, M. Tehranipoor, S. Bhunia, and F. Forte, **Introduction to Hardware Obfuscation: Motivation, Methods and Evaluation** in *Hardware Protection through Obfuscation*, 2017.
12. Q. Shi, D. Forte and M. Tehranipoor, **Analyzing Circuit Layout to Probing Attack**, in *Hardware IP Security and Trust: Validation and Test*, 2017.
13. A. Nahiyani and M. Tehranipoor, **Code Coverage Analysis for IP Trust Verification**, in *Hardware IP Security and Trust: Validation and Test*, 2017.
14. H. Salmani and M. Tehranipoor, **Digital Circuits Vulnerability to Hardware Trojans**, in *Hardware IP Security and Trust: Validation and Test*, 2017.
15. A. Nahiyani, K. Xiao, D. Forte, and M. Tehranipoor, **Security Rule Check**, in *Hardware IP Security and Trust: Validation and Test*, 2017.
16. P. Mishra, S. Bhunia, and M. Tehranipoor, **Security and Trust Vulnerabilities in Third-Party IPs**, in *Hardware IP Security and Trust: Validation and Test*, 2017.
17. P. Mishra, S. Bhunia, and M. Tehranipoor, **The Future of Trustworthy Design**, in *Hardware IP Security and Trust: Validation and Test*, 2017.
18. K. Xiao, D. Forte, and M. Tehranipoor, **Circuit Timing Signature (CTS) for Detection of Counterfeit Integrated Circuits**, in *Secure System Design and Trustable Computing*, by *Chip Hong Chang and Miodrag Potkonjak*, 2014.
19. M. Tehranipoor and J. Lee, **Protecting IPs Against Scan-Based Side-Channel Attacks**, in *Introduction to Hardware Security and Trust*, Springer, March 2011.

20. M. Tehranipoor and J. Lee, **Protecting IPs Against Scan-Based Side-Channel Attacks**, in *Introduction to Hardware Security and Trust*, Springer, March 2011.
21. M. Tehranipoor, **Built-In Self-Test and Defect Tolerance for Molecular Electronics-Based NanoFabrics**, in *Robust Nano-Computing* by Chao Huang, Springer 2010.
22. M. Tehranipoor and B. Sunar, **Hardware Trojan Horses**, in *Towards Hardware Intrinsic Security: Foundation and Practice*, by Ahmad R. Sadeghi, Springer, 2010.
23. M. Tehranipoor and N. Ahmed, **Faster-than-at-speed Test for Detecting SDDs**, in *Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits* by S. Sandeep Goel and K. Chakrabarty, 2010.
24. K. Peng, M. Yilmaz, and M. Tehranipoor, **Path-Grading Considering Layout, Process Variations, and Crosstalk**, in *Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits* by S. Sandeep Goel and K. Chakrabarty, 2010.
25. M. Kassab and M. Tehranipoor, **Test for Power Management Systems**, in *Low Power Testable Design* by P. Girard, N. Nicolici, and X. Wen, Springer, 2009.
26. M. Tehranipoor, **Test and Defect Tolerance for Nanoscale Crossbar-based Circuits**, in *System on Chip Test Architectures: Nanometer Design for Testability*, by L.T. Wang, Charles Stroud and Nur Touba, Elsevier, Target Publication Date: Oct. 2007.
27. M. Tehranipoor and R. Rad, **Defect Tolerance for Reconfigurable Nanoscale Architectures**, in *Emerging Nanotechnologies: Test, Defect Tolerance, and Reliability*, by M. Tehranipoor, Springer, 2007.

Patents

1. **Embedded ring oscillator network for integrated circuit security and threat detection**, 2014, M. Tehranipoor, X. Wang, X. Zhang, US 8850608 B2, WO 2012122309 A3 (**Grant**)
2. **Methods and Systems for Hardware Piracy Prevention**, 2014, M. Tehranipoor and N. Tuzzio, US9071428 B2 (**Grant**)
3. **Methods and Systems for Preventing Hardware Trojan Insertion**, M. Tehranipoor and K. Xiao, US20140283147 A1 (**Grant**)
4. **Photon-Counting Security Tagging and Verification Using Optically Encoded QR Codes**, B. Javidi, A. Markman, and M. Tehranipoor, US20150295711 A1 (**Grant**)
5. **Detection of Recovered Integrated Circuits**, 2014, M. Tehranipoor, N. Tuzzio, and X. Zhang, US 2014/0340112 A1, Publication number: 20140103344 (Application)
6. **Methods and Systems for Test Power Analysis**, 2014, M. Tehranipoor and W. Zhao, US20140365148 A1, Publication number: 20140365148 (Application)
7. **Circuit Edit and Obfuscation for Trusted Chip Fabrication**, 2016, M. Tehranipoor, D. Forte, and B. Shakya (Application)
8. **FORTIS: Establishing Forward Trust for Protecting IPs and ICs in Today's Complex Supply Chain**, 2016, M. Tehranipoor, D. Forte, and U. Guin (Application)
9. **UCR: An Unclonable Environmentally-Sensitive Chipless RFID Tag**, 2016, M. Tehranipoor, D. Forte, K. Yang, and H. Shen (Application)

10. **Layout-Driven Method to Assess Vulnerability of ICs to Microprobing Attacks**, 2017, M. Tehranipoor, D. Forte, N. Asadi, and Q. Shi (UF#16487; SLE ref. UF.1293P)
11. **Vanishing Via for Hardware IP Protection Against Reverse Engineering**, 2017, S. Bhunia, M. Tehranipoor, D. Forte, N. Asadi, and H. Shen (UF# 1294)
12. **Eco-system of Security Vulnerability Assessment from RTL to Layout**, G. Contreras, S. Bhunia, and M. Tehranipoor, Work Disclosure
13. **Side-channel Leakage Analysis for Power, EM, Fault, and Timing**, S. Bhunia, M. Tehranipoor, and Jungmin Park
14. **Micro-probing Vulnerability Analysis**, M. Tehranipoor, D. Fote and Q. Shi
15. **SecureHDL Framework for Vulnerability Analysis**, S. Bhunia, G. Contreras, D. Capecci, H. Wang, and M. Tehranipoor

Guest Editorials

1. S. Bhunia and M. Tehranipoor, First Ever Issue of HaSS Journal, Journal of Hardware and Systems Security (HaSS), March 2017.
2. S. Hu, Y. Jin, K. Heffner, and M. Tehranipoor, **Hardware/Software Cross-Layer Technologies for Trustworthy and Secure Computing**, IEEE TMSCS, 2016.
3. I. Polian and M. Tehranipoor, Special Issue on **Hardware Security**, Guest Editorial, IET Computers and Digital Techniques, 2015.
4. M. Tehranipoor and F. Koushanfar, "**Hardware Security and Trust**," Guest Editorial, IEEE Computer Society Computing Now (CN), September 2010.
5. M. Tehranipoor and F. Koushanfar, "**Confronting the Hardware Trustworthiness Problem**," Guest Editorial, IEEE Design and Test of Computers, Jan 2010.
6. M. Tehranipoor and K. Butler, "**IR-Drop and Power Supply Noise Effects on Design and Test of Very Deep Submicron Designs**," Guest Editorial, IEEE Design and Test of Computers, July 2007.
7. M. Tehranipoor, "**Test, Defect Tolerance and Reliability of Nanoscale Devices**," Guest Editorial, Journal of Electronic Testing: Theory and Applications (JETTA), Vol. 23, No. 2/3, pp. 115-116, June 2007.

Edited Conference Proceedings

1. S. Menon and M. Tehranipoor, Proceedings for IEEE Defect-Based Testing (**DBT**) Workshop, 2007.
2. N. Ahmed and M. Tehranipoor, Proceedings for IEEE Defect and Data Driven Testing (**D3T**) Workshop, 2008.
3. N. Ahmed and M. Tehranipoor, Proceedings for IEEE Defect and Data Driven Testing (**D3T**) Workshop, 2009.
4. D. Gizopolous, M. Tehranipoor, S. Tragoudas, Proceedings for IEEE Symposium on Defect and Fault Tolerance in VLSI Systems (**DFTS**), 2008.
5. D. Gizopolous, M. Tehranipoor, S. Tragoudas, Proceedings for IEEE Symposium on Defect and Fault Tolerance in VLSI Systems (**DFTS**), 2009.
6. J. Plusquellic and M. Tehranipoor, Proceedings for IEEE Symposium on Hardware-Oriented Security and Trust (**HOST**), 2008.

7. J. Plusquellic and M. Tehranipoor, Proceedings for IEEE Symposium on Hardware-Oriented Security and Trust (**HOST**), 2009.

Journal Papers

1. K. Yang, D. Forte, and M. Tehranipoor, “**ReSC: An RFID-Enabled Solution for Defending IoT Supply Chain**,” ACM Transactions on Design Automation of Electronic Systems (**TODAES**), 2017.
2. M. Alam, S. Choudhury, B. Park, D. Munzer, N. Maghari, M. Tehranipoor, and D. Forte, “**Challenges and Opportunities in Analog and Mixed Signal (AMS) Integrated Circuit (IC) Security**,” Journal of Hardware and Systems Security (**HaSS**), 2017.
3. Z. Guo, X. Xu, T. Rahman, M. Theranipoor, and D. Forte, “**SCARe: An SRAM based Countermeasure Against IC Recycling Framework**,” IEEE Transactions on VLSI (**TVLSI**), 2017.
4. M. Alam, M. Tehranipoor, and U. Guin, “**TSensors Vision, Infrastructure, and Security Challenges in Trillion Sensor Era**,” Journal of Hardware and Systems Security (**HaSS**), 2017.
5. X. Wang, D. Zhang, M. He, and M. Tehranipoor, “**Secure Scan and Test Using Obfuscation Throughout Supply Chain**,” IEEE Transactions on Computer-Aided Design (**TCAD**), 2017.
6. E. Principe, N. Asadi, D. Forte, R. Chivas, M. DiBattista, and S. Silverman, “**Plasma FIB Deprocessing of Integrated Circuits from the Backside**,” Electronic Device Failure Analysis (**EDFA**), 2017.
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Conference Papers

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14. X. Wang, Y. Guo, T. Rahman, D. Zhang, and M. Tehranipoor, "**DOST: Dynamically Obfuscated Wrapper for Split Test against IC Piracy**," IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2017. **Received Best Paper Award.**
15. Z. Guo, X. Xu, M. Tehranipoor, and D. Forte, "**MPA: Model-assisted PCB Attestation via Board-level RO and Temperature Compensation**," IEEE Asian Hardware-Oriented Security and Trust Symposium (AsianHOST), 2017.
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35. Z. Guo, M. Tehranipour, and D. Forte, "**Aging Attacks for Key Extraction on Permutation-Based Obfuscation**," IEEE Asian Hardware-Oriented Security and Trust (AsianHOST), 2016.
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56. K. Yang, D. Forte, and M. Tehranipoor, "**UCR: An Unclonable Chipless RFID Tag**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016.
57. Q. Shi, N. Asadi, D. Forte, and M. Tehranipoor, "**A Layout-driven Framework to Assess Vulnerability of ICs to Microprobing Attacks**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016. **(Best Paper Award)**
58. Z. Guo, T. Rahman, M. Tehranipoor, and D. Forte, "**A Zero-cost Approach to Detect Recycled SoC Chips Using Embedded SRAM**," IEEE Symposium on Hardware-Oriented Security and Trust (HOST), 2016. **(Best Paper Nominate)**

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113. J. Chen, L. Winemberg, and M. Tehranipoor, "**Identification of Testable Representative Paths for Low-Cost Verification of Circuit Performance During Manufacturing Tests and in the Field**," IEEE VLSI Test Symposium (VTS), 2014.
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121. J. Chen and M. Tehranipoor, "**Critical Paths Selection and Test Cost Reduction Considering Process Variations**," IEEE Asian Test Symposium (ATS), pp. 259 - 264, 2013.
122. F. Bao, H. Chen, and M. Tehranipoor, "**Worst-case Critical-Path Delay Analysis Considering Power-Supply Noise**," IEEE Asian Test Symposium (ATS), pp. 37-42, 2013.
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125. U. Guin, D. DiMase, and M. Tehranipoor, "**CDC: Counterfeit Defect Coverage Analysis**," DMSMS, 2013 (Invited)
126. A. Mazady, H. Chi Chou, M. Tehranipoor and M. Anwar, "**Terahertz Spectroscopy: A Technology Platform for the Detection of Counterfeit Electronics**," DMSMS, 2013 (Invited)
127. U. Guin, T. Chakraborty, and M. Tehranipoor, "**Novel DFTs for Circuit Initialization to Reduce Functional Fmax Test Time**," IEEE Int. Conference on Computer Design (ICCD), 2013. ??

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157. M. Tehranipoor and N. Bidokhti, “**Timing Analysis and On-Chip Measurement Considering Aging**,” IEEE Int. Reliability Innovations Conference (IRIC), 2012 (*Extended Abstract*).
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167. W. Zhao and M. Tehranipoor, "**Peak Power Identification on Power Bumps During Test Application**," Low Power SOC Workshop (LPSOC), pp. 1-3, 2011 (*Invited*).
168. X. Zhang and M. Tehranipoor, "**Case Study: Detecting Hardware Trojans in Third-Party Digital IP Cores**," Int. IEEE Hardware-Oriented Security and Trust (HOST), pp. 67-70, 2011.
169. F. Bao, K. Peng, M. Yilmaz, K. Chakrabarty, and M. Tehranipoor, "**Critical Fault-Based Pattern Generation for Screening Small Delay Defects**," in proc. European Test Symposium (ETS), pp. 1177-182, 2011.
170. S. Wang and M. Tehranipoor, "**Aging Measurement and Calibration for Nanoscale VLSI Circuit**," Connecticut Symposium on Microelectronics and Optoelectronics (CMOC), 2011 (*Invited*).
171. J. Chen and M. Tehranipoor, "**Timing Analysis for Nanometer VLSI Designs Considering Aging Effects**," Connecticut Symposium on Microelectronics and Optoelectronics (CMOC), 2011 (*Poster*).
172. X. Zhang and M. Tehranipoor, "**RON: An On-chip Ring Oscillator Network for Hardware Trojan Detection**," Design, Automation, and Test in Europe (DATE), pp. 1-6, 2011.
173. F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipoor, K. Miyase, X. Wen, and N. Ahmed, "**Power Reduction Through X-filling of Transition Fault Test Vectors for LOS Testing**," in Design & Technology of Integrated Systems (DTIS), pp. 1-6, 2011.
174. W. Zhao, S. Chakravarty, and M. Tehranipoor, "**Power-Safe Test Application Using An Effective Gating Approach Considering Current Limits**," IEEE VLSI Test Symposium (VTS), pp. 160-165, 2011.
175. K. Peng, F. Bao, G. Shofner, L. Winemberg, and M. Tehranipoor, "**Case Study: Efficient SDD Test Generation for Very Large Integrated Circuits**," IEEE VLSI Test Symposium (VTS), pp. 78-83, 2011.

176. J. Ma, N. Ahmed, and M. Tehranipoor, "**Low-Cost Diagnostic Pattern Generation and Evaluation Procedures for Noise-Related Failures**," IEEE VLSI Test Symposium (VTS), pp. 309-314, 2011.
177. X. Wen, K. Enokimoto, K. Miyase, Y. Yamato, M. Kochte, S. Kajihara, P. Girard, M. Tehranipoor, "**Power-Aware Test Generation with Guaranteed Launch Safety for At-Speed Scan Testing**," IEEE VLSI Test Symposium (VTS), pp. 166-171, 2011.
178. M. Tehranipoor, "**Verifying Trustworthiness of Integrated Circuits**," GOMACTech, 2011 (*Invited*).
179. J. Chen, S. Wang, N. Bidokhti, and M. Tehranipoor, "**A Framework for Fast and Accurate Critical-Reliability Paths Identification**," IEEE North Atlantic Test Workshop (NATW), 2011.
180. F. Bao, K. Peng, K. Chakrabarty, L. Winemberg, and M. Tehranipoor, "**Increasing SDD Coverage without Increasing Pattern Count**," IEEE North Atlantic Test Workshop (NATW), 2011.
181. N. Reddy, S. Wang, L. Winemberg, and M. Tehranipoor, "**Experimental Analysis for Aging in Integrated Circuits**," IEEE North Atlantic Test Workshop (NATW), 2011.
182. J. Ma, M. Tehranipoor, O. Sinanoglu, and S. Almkhaizim, "**Identification of IR-drop Hot-spots in Defective Power Distribution Network Using TDF ATPG**," Int. Workshop on Design and Test (IDT), pp. 122-127, 2010.
183. M. Tehranipoor, "**Dealing with Reliability and Variability Issues in Nanometer Technology Designs**," Connecticut Symposium on Microelectronics and Optoelectronics (CMOC), 2010 (*Invited*).
184. H. Salmani, M. Tehranipoor, and J. Plusquellic, "**A Layout-Aware Approach for Improving Localized Switching to Detect Hardware Trojans in Integrated Circuits**," IEEE International Workshop on Information Forensics and Security (WIFS), pp. 1-6, 2010.
185. W. Zhao, J. Ma, M. Tehranipoor, and S. Chakravarty, "**Power-Safe Application of Transition Delay Fault Patterns Considering Current Limit during Wafer Test**," IEEE Asian Test Symposium (ATS), pp. 301-306, 2010.
186. K. Peng, M. Yilmaz, K. Chakrabarty, and M. Tehranipoor, "**A Noise-Aware Hybrid Method for SDD Pattern Grading and Selection**," IEEE Asian Test Symposium (ATS), pp. 331-336, 2010.
187. S. Goel, K. Chakrabarty, M. Yilmaz, K. Peng, and M. Tehranipoor, "**Circuit Topology-Based Test Pattern Generation for Small-Delay Defects**," IEEE Asian Test Symposium (ATS), pp. 307-312, 2010.
188. F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipoor, J. Ma, W. Zhao, X. Wen, "**Analysis of Power Consumption and Transition Fault Coverage for LOS and LOC Testing Schemes**," DDECS, pp. 376-381, 2010.
189. X. Wang and M. Tehranipoor, "**Low-Cost On-Chip Structures for Measuring NBTI Effects, Variations, Path Delay, and Noise**," SRC TECHCON, Poster Presentation, 2010.
190. F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipoor, K. Miyase, X. Wen, and N. Ahmed, "**Power reduction Through X-filling of Transition Fault Vectors for LOS Testing**," International Workshop on the Impact of Low Power design on Test and Reliability (LPonTR), pp. 1-6, 2010.
191. J. Ma and M. Tehranipoor, "**A Low-Cost Diagnostic Procedure for Parametric Failures Caused by Pattern-Induced Noises**," SRC TECHCON, Poster Presentation, 2010.

192. K. Peng, Y. Huang, W. T. Cheng, and M. Tehranipour, "**Full-Circuit SPICE Simulation Based Validation of Dynamic Delay Estimation**," European Test Symposium (ETS), pp. 101-106, 2010.
193. J. Ma, J. Lee, N. Ahmed, P. Girard, and M. Tehranipour, "**Pattern Grading for Testing Critical Paths Considering Power Supply Noise and Crosstalk Using a Layout-Aware Quality Metric**," Great-Lake Symposium on VLSI (GLS-VLSI), pp. 127-130, 2010.
194. K. Peng, J. Thibodeau, M. Yilmaz, K. Chakrabarty, and M. Tehranipour, "**A Novel Hybrid Method for SDD Pattern Grading and Selection**," IEEE VLSI Test Symposium (VTS), pp. 45-50, 2010.
195. K. Peng, M. Yilmaz, K. Chakrabarty, and M. Tehranipour, "**High-Quality Pattern Selection for Screening Small-Delay Defects Considering Process Variations and Crosstalk**," Design, Automation, and Test in Europe (DATE), pp. 1426-1431, 2010.
196. X. Wang and M. Tehranipour, "**Novel Physical Unclonable Function Based on Process and Environmental Variations**," Design, Automation, and Test in Europe (DATE), pp. 1065-1070, 2010.
197. K. Peng, Y. Huang, R. Guo, W. T. Cheng, and M. Tehranipour, "**Emulating and Diagnosing IR-Drop by Using Dynamic SDF**," ASP-DAC, pp. 511-516, 2010.
198. X. Wang, M. Tehranipour, and R. Datta, "**A Novel Architecture for On-Chip Path Delay Measurement**," International Test Conference (ITC), pp. 1-10, 2009.
199. J. Ma, J. Lee, and M. Tehranipour, "**Extended Abstract: Developing a Novel Quality Metric for Path-Delay Fault Pattern Evaluation**," IEEE Int. Workshop on Defect and Data Driven Testing (D3T), 2009.
200. K. Peng, Y. Huan, W. T. Cheng, and M. Tehranipour, "**Efficient Modeling of IR-Drop Using Dynamic SDF for Test and Diagnosis**," IEEE Workshop on RTL and High Level Testing (WRTL), 2009.
201. K. Peng, M. Yilmaz, K. Chakrabarty, and M. Tehranipour, "**Efficient Pattern Grading for Small Delay Defects in Digital Integrated Circuits**," IEEE North Atlantic Test Workshop, May 2009 **(Received Best Paper Award)**.
202. H. Salmani, M. Tehranipour, and J. Plusquellic, "**New Design Strategy for Improving Hardware Trojan Detection and Reducing Trojan Activation Time**," IEEE Workshop on Hardware-Oriented Security and Trust (HOST), pp. 67-73, 2009.
203. J. Ma, J. Lee, and M. Tehranipour, "**Layout-Aware Pattern Generation for Maximizing Supply Noise Effects on Critical Paths**," in Proc. IEEE VLSI Test Symposium (VTS), pp. 221-226, 2009.
204. J. Ma, J. Lee, and M. Tehranipour, "**Layout-Aware Pattern Generation for Critical Paths Considering Supply Voltage Noise**," Poster Presentation, SRC TECHCON, Austin, TX, 2009 **(Received Best in Session Award)**.
205. H. Furukawa, X. Wen, K. Miyase, Y. Yamoto, S. Kajihara, P. Girard, L.T. Wang, M. Tehranipour, "**CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme for Reducing Yield Loss Risk in At-Speed Testing**," IEEE Asian Test Symposium (ATS), pp. 197-402, 2008.
206. M. tehranipour, "**ATPG for Increased Test Quality and In-Field Reliability**," DRV Workshop, 2008 (Invited).

207. J. Ma, J. Lee, M. Tehranipoor, X. Wen, A. Crouch, "**Identification of IR-drop Hot-spots in Defective Power Distribution Network Using TDF ATPG**," in Proc. Int. Workshop on Defect and Data Driven Testing (**D3T**), 2008.
208. X. Wang, M. Tehranipoor, and R. Datta, "**Path-RO: A Novel On-Chip Critical Path Delay Measurement Under Process Variations**," International Conference on Computer-Aided Design (**ICCAD**), pp. 640-646, 2008.
209. R. Rad, X. Wang, J. Plusquellic, and M. Tehranipoor, "**Taxonomy of Trojans and Methods of Detection for IC Trust**," International Conference on Computer-Aided Design (**ICCAD**), Nov. 2008.
210. X. Wang, H. Salmani, M. Tehranipoor, and J. Plusquellic, "**Hardware Trojan Detection and Isolation Using Current Integration and Localized Current Analysis**," International Symposium on Fault and Defect Tolerance in VLSI Systems (**DFT**), pp. 87-95, Oct. 2008.
211. X. Wang, M. Tehranipoor, and R. Datta "**Accurate On-Chip Path Delay Measurement**," Texas Instruments Symposium on Test (**TIST**), Aug. 2008
212. J. Lee and M. Tehranipoor, "**A Novel Test Pattern Generation Framework for Inducing Maximum Crosstalk Effects on Delay-Sensitive Paths**," IEEE International Test Conference (**ITC**), pp. 1-10, Oct. 2008.
213. M. Yilmaz, K. Chakrabarty and M. Tehranipoor, "**Interconnect-Aware and Layout-Oriented Test-Pattern Selection for Small-Delay Defects**," IEEE International Test Conference (**ITC**), pp. 1-10, Oct. 2008.
214. J. Ma, J. Lee, and M. Tehranipoor, "**Power Distribution Failure Analysis Using Transition-Delay Fault Pattern Generation**," Poster presentation at IEEE International Test Conference (**ITC**), Oct. 2008.
215. X. Wang, M. Tehranipoor, and R. Datta "**Path-RO: On-Chip Critical Path Delay Measurement Under Process Variations**," IEEE North Atlantic Test Workshop (**NATW**), May 2008 (**Received Best Paper Award**).
216. J. Ma, J. Lee, M. Tehranipoor, and A. Crouch "**Test Pattern Generation for Open Defects in Power Distribution Networks**," IEEE North Atlantic Test Workshop (**NATW**), May 2008.
217. J. Lee, S. Narayan, and M. Tehranipoor, "**Low-Power Transition-Delay Fault Pattern Generation**," IEEE North Atlantic Test Workshop (**NATW**), May 2008 (**Received Honorable Mention for Best Paper Award**).
218. X. Wang, M. Tehranipoor, and J. Plusquellic, "**Detecting Malicious Inclusions in Secure Hardware: Challenges and Solutions**," IEEE Int. Hardware-Oriented Security and Trust (**HOST**), pp. 15-19, 2008.
219. R. Rad, J. Plusquellic, and M. Tehranipoor, "**Sensitivity Analysis to Hardware Trojans using Power Supply Transient Signals**," IEEE Int. Hardware-Oriented Security and Trust (**HOST**), pp. 3-7, 2008.
220. J. Lee and M. Tehranipoor, "**LS-TDF: Low Switching Transition Delay Fault Test Pattern Generation**," in Proc. IEEE VLSI Test Symposium (**VTS**), pp. 227-232, 2008.
221. M. Yilmaz, K. Chakrabarty, and M. Tehranipoor, "**Test Grading and Pattern Selection for Small Delay Defects**," in Proc. IEEE VLSI Test Symposium (**VTS**), pp. 233-239, 2008.
222. J. Lee, S. Narayan, M. Kapralos, and M. Tehranipoor, "**Layout-aware, IR-drop Tolerant Transition Fault Pattern Generation**," in Proc. Design, Automation, and Test in Europe (**DATE**), pp. 1172-1177, 2008.

223. J. Lee, K. Peng, and M. Tehranipoor, "**Inducing Maximum Crosstalk Effects on Delay-Sensitive Paths**," Poster presentation, SRC TECHCON, Austin, TX, 2008.
224. M. Yilmaz, K. Chakrabarty and M. Tehranipoor, "**Test Pattern Grading for Small Delay Defects**," Int. Workshop on Defect-Based Testing (DBT'07), 2007.
225. R. Helinski, J. Plusquellic and M. Tehranipoor, "**Small Delay Defect Detection Using Self-Relative Timing Bounds**," Int. Workshop on Defect-Based Testing (DBT'07), 2007.
226. J. Lee and M. Tehranipoor, "**Delay Fault Testing in Presence of Maximum Crosstalk**," 16th IEEE North Atlantic Test Workshop (NATW'07), Boxborough, MA, 2007.
227. N. Ahmed, M. Tehranipoor and V. Jayaram, "**IR-drop Tolerant Transition Delay Fault Testing**," 16th IEEE North Atlantic Test Workshop (NATW'07), Boxborough, MA, 2007.
228. N. Ahmed, M. Tehranipoor and V. Jayaram, "**Transition Delay Fault Test Pattern Generation Considering Supply Voltage Noise in a SOC Design**," in Proc. Design Automation Conference (DAC'07), pp. 533-538, 2007.
229. N. Ahmed, M. Tehranipoor and V. Jayaram, "**Supply Voltage Noise Aware ATPG for Transition Delay Faults**," in Proc. IEEE VLSI Test Symposium (VTS'07), pp. 179-186, 2007.
230. N. Ahmed and M. Tehranipoor, "**Supply Voltage Noise Aware ATPG for Transition Delay Faults**," TECHCON, Austin, TX 2007.
231. N. Ahmed, M. Tehranipoor and V. Jayaram, "**Improving ATPG and Pattern Selection for Screening Small Delay Defects**," IEEE Int. Workshop on Current and Defect Based Testing (DBT'06), 2006.
232. J. Plusquellic, D. Acharyya, A. Singh, M. Tehranipoor and C. Patel, "**Multiple Supply Pad IDDQ_based Defect Detection Techniques Applied to Hardware Test Chips**," IEEE Int. Workshop on Current and Defect Based Testing (DBT'06), 2006.
233. J. Plusquellic, D. Acharyya, A. Singh, M. Tehranipoor and C. Patel, "**Triangulating to a Defect's Physical Coordinates Using Multiple Supply Pad IDDQs: Test Chip Results**," in Proc. International Symposium for Testing and Failure Analysis Conference (ISTFA'06), pp. 36-42, 2006.
234. N. Ahmed, M. Tehranipoor and V. Jayaram, "**A Novel Framework for Faster-than-at-Speed Delay Test Considering IR-Drop Effects**," in Proc. Int. Conf. on Computer-Aided Design (ICCAD'06), pp. 198-203, 2006.
235. R. M. Rad and M. Tehranipoor, "**A Hybrid FPGA Using Nanoscale Cluster and CMOS Scale Routing**," in Proc. Design Automation Conference (DAC'06), pp. 727-730, 2006.
236. N. Ahmed, M. Tehranipoor and V. Jayaram, "**Timing-Based Delay Test for Screening Small Delay Defects**," in Proc. Design Automation Conference (DAC'06), pp. 320-325, 2006 (**Best Paper Award Candidate**).
237. R. M. Rad and M. Tehranipoor, "**A Reconfiguration-based Defect Tolerance Method for Nanoscale Devices**," in Proc. Int. Symposium on Defect and Fault Tolerance of VLSI Systems (DFT'06), pp. 107-118, 2006.
238. R. M. Rad and M. Tehranipoor, "**SCT: An Approach for Testing and Configuring Nanoscale Devices**," in Proc. IEEE VLSI Test Symposium (VTS'06), pp. 372-377, 2006.
239. J. Lee, M. Tehranipoor and J. Plusquellic, "**A Low-Cost Solution for Protecting IPs Against Side-Channel Scan-Based Attacks**," In Proc. IEEE VLSI Test Symposium (VTS'06), pp. 94-99, 2006.

240. R. M. Rad and M. Tehranipoor, "**Test Time and Defect Map Analysis of PLA and LUT-Based Nano-Architectures**," IEEE North Atlantic Test Workshop (NATW'06), 2006.
241. N. Ahmed, M. Tehranipoor and V. Jayaram, "**A Case Study of IR-Drop Effects during Faster-than-at-Speed Delay Test**," IEEE North Atlantic Test Workshop (NATW'06), 2006.
242. J. Plusquellic, D. Acharyya, A. Singh, M. Tehranipoor and C. Patel, "**Triangulating to a Defect's Physical Coordinates Using Multiple Supply Pad IDDQs: Test Chip Results**," IEEE North Atlantic Test Workshop (NATW'06), 2006.
243. J. Lee, N. Ahmed, M. Tehranipoor, V. Jayaram and J. Plusquellic, "**A Novel Framework for Functionally Untestable Transition Fault Avoidance during ATPG**," IEEE North Atlantic Test Workshop (NATW'06), 2006.
244. R. M. P. Rad and M. Tehranipoor, "**Fine-Grained Island Style Architecture for Molecular Electronic Devices**," International Symposium on Field-Programmable Gate Arrays (FPGA'06) (Poster), pp. 226, 2006.
245. M. Tehranipoor and R. M. P. Rad, "**Test and Recovery for Fine-Grained Nanoscale Architectures**," International Symposium on Field-Programmable Gate Arrays (FPGA'06) (Poster), 2006.
246. M. ElShoukry, C.P. Ravikumar and M. Tehranipoor, "**Partial Gating Optimization for Power Reduction During Test Application**," in Proc. IEEE Asian Test Symposium (ATS'05), pp. 242-247, 2005.
247. M. Tehranipoor, M. Nourani and N. Ahmed, "**Low Transition LFSR for BIST-Based Applications**," in Proc. IEEE 14th Asian Test Symposium (ATS'05), pp. 138-143, 2005.
248. C.P. Ravikumar, N. Ahmed and M. Tehranipoor, "**Practicing Transition-Fault Testing with Physical-Design-Friendly Flows**," Texas Instruments India Technical Conference (TIITC'05), 2005.
249. J. Lee, M. Tehranipoor, C. Patel and J. Plusquellic, "**Securing Scan Design Using Lock & Key Technique**," in Proc. International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'05), pp. 51-62, 2005.
250. N. Ahmed and M. Tehranipoor, "**Improving Transition Delay Fault Coverage Using Hybrid Scan-Based Technique**," in Proc. International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'05), 2005.
251. M. Tehranipoor, "**Defect Tolerance for Molecular Electronics-Based NanoFabrics Using Built-In Self-Test Procedure**," in Proc. International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'05), pp. 4886-495, 2005.
252. M. Alisafae, S. M. Fakhraie and M. Tehranipoor, "**Architecture of an Embedded Queue Management Engine for High-Speed Network Devices**," in Proc. IEEE MidWest Symposium on Circuits and Systems (MWSCAS'05), Cincinnati, pp. 1907-1910, 2005.
253. H. Esmailzadeh, F. Farzan, N. Shahidi, S. M. Fakhraie, C. Lucas and M. Tehranipoor, "**NnSP: Embedded Neural Networks Stream Processor**," in Proc. IEEE MidWest Symposium on Circuits and Systems (MWSCAS'05), Cincinnati, pp. 223-226, 2005.
254. N. Ahmed, M. Tehranipoor and C.P. Ravikumar, "**Addressing At-speed Fault Coverage and Test Cost Issues Using Enhanced Launch-off-Capture**," Texas Instruments Symposium on Test (TIST'05), 2005.

255. N. Ahmed, M. Tehranipour and C.P. Ravikumar, "**At-Speed Local Scan Enable Generation for Transition Fault Testing Using Low-Cost Testers**," Texas Instruments Symposium on Test (TIST'05), 2005 (**Ranked 5th Among 89 Presentations**).
256. N. Ahmed, M. Tehranipour and C.P. Ravikumar, "**Enhanced Launch-off-Capture Transition Fault Testing**," in Proc. IEEE International Test Conf. (ITC'05), pp. 225-234, 2005 (**Received top ten recognition**).
257. N. Ahmed, M. Tehranipour, C.P. Ravikumar and J. Plusquellic, "**At-Speed Transition Fault Testing Using Low Speed Testers With Application to Reduced Scan Enable Routing Area**," IEEE North Atlantic Test Workshop (NATW'05), pp. 112-119, 2005.
258. D. Acharyya, A. Singh, M. Tehranipour, C. Patel and J. Plusquellic, "**Sensitivity Analysis of Quiescent Signal Analysis for Defect Detection**," IEEE. Int. Workshop on Defect Based Testing (DBT'05), pp. 3-10, 2005.
259. M. Nourani, M. Tehranipour and N. Ahmed, "**Pattern Generation and Estimation for Power Supply Noise Analysis**," in proc. IEEE VLSI Test Symposium (VTS'05), pp. 439-444, 2005.
260. N. Ahmed, C.P. Ravikumar, M. Tehranipour and J. Plusquellic, "**At-Speed Transition Fault Testing With Low Speed Scan Enable**," in proc. IEEE VLSI Test Symposium (VTS'05), pp. 42-47, 2005 (**Received Best Paper Award**).
261. M. H. Tehranipour, M. Nourani and K. Chakrabarty, "**Nine-Coded Compression Technique with Application to Reduced Pin-Count Testing and Flexible On-Chip Decompression**," in proc. IEEE/ACM Design, Automation and Test in Europe (DATE'04), Paris, France, vol. 2, pp. 1284-1289, 2004.
262. M. H. Tehranipour, M. Nourani, K. Arabi and A. Afzali-Kusha, "**Mixed RL-Huffman Encoding for Power Reduction and Data Compression in Scan Test**," in proc. IEEE International Symposium on Circuits And Systems (ISCAS'04), Vancouver, Canada, vol. 2, pp. 681-684, 2004.
263. N. Ahmed, M. H. Tehranipour and M. Nourani, "**Low-Power Pattern Generation for BIST Architecture**," in proc. IEEE International Symposium on Circuits And Systems (ISCAS'04), Vancouver, Canada, vol. 2, pp. 689-692, 2004.
264. N. Ahmed, M. H. Tehranipour, D. Zhou and M. Nourani, "**Frequency Driven Repeater Insertion for Deep Submicron**," in proc. IEEE International Symposium on Circuits And Systems (ISCAS'04), Vancouver, Canada, vol. 5, 181-184, 2004.
265. M. H. Tehranipour, N. Ahmed and M. Nourani, "**Testing SoC Interconnects for Signal Integrity Using Boundary Scan**," in proc. IEEE VLSI Test Symposium (VTS'03), Napa, CA, pp. 158-163, 2003.
266. N. Ahmed, M. H. Tehranipour and M. Nourani, "**Extending JTAG for Testing Signal Integrity in SoCs**," in proc. IEEE/ACM Design, Automation and Test in Europe (DATE'03), Messe Munich, Germany, pp. 218-223, 2003.
267. M. H. Tehranipour, N. Ahmed and M. Nourani, "**Multiple Transition Model and Enhanced Boundary Scan Architecture to Test Interconnects for Signal Integrity**," in proc. IEEE International Conference on Computer Design (ICCD'03), San-Jose, pp. 554-559, CA, 2003.
268. M. H. Tehranipour, M. Nourani and S. M. Fakhraie, "**Systematic Test Program Generation for SoC Testing Using Embedded Processor**," in proc. IEEE International Symposium on Circuits And Systems (ISCAS'03), Bangkok, Thailand, vol. 5, pp. 541-544, 2003.

269. G. R. Chaji, R. M. Pourrad, S. M. Fakhraie and M. H. Tehranipour, “**eUTDSP: A Design Study of a New VLIW-Based DSP Architecture**,” in proc. IEEE International Symposium on Circuits And Systems (ISCAS'03), Bangkok, Thailand, vol. 4, pp. 137-140, 2003.
270. M. H. Tehranipour and M. Nourani, “**Signal Integrity Loss in SoC's Interconnects: A Diagnostic Approach Using Embedded Microprocessor**,” in proc. IEEE International Test Conference (ITC'02), Baltimore, MD, pp.1093-1102, 2002.
271. S. M. Fakhraie, M. H. Tehranipour, M. R. Movahedin and M. Nourani, “**Fast Prototyping of a DSP Core**,” in proc. IEEE MidWest Symposium on Circuits and Systems (MWSCAS'02), Tulsa, Oklahoma, vol. 2, pp. 215-218, 2002.
272. M. H. Tehranipour, M. Nourani, S. M. Fakhraie and C. A. Papachristou, “**Test Optimization of Bus-Structured SoCs Using Embedded Microprocessor**,” in proc. IEEE MidWest Symposium on Circuits and Systems (MWSCAS'02), Tulsa, Oklahoma, vol. 1, pp. 168-171, 2002.
273. M. Tehranipour, Z. Navabi and S. M. Fakhraie, “**An Efficient BIST for Embedded SRAM Testing**,” in proc. IEEE International Symposium on Circuits And Systems (ISCAS'01), Sydney, Australia, Vol 5, pp. 73-76, 2001.
274. M. Tehranipour, Z. Navabi and S. M. Fakhraie, “**A Low-Cost BIST Architecture for Processor Cores**,” in proc. IEEE Electronic Circuits and Systems Conference (ECS'01), Bratislava, Slovakia, pp. 11-14, 2001.
275. M. Tehranipour and Z. Navabi, “**Zero-Overhead BIST for Internal SRAM Testing**,” in proc. IEEE International Conference on Microelectronics (ICM'00), Tehran, Iran, pp. 109-112, 2000.

Technical Reports and Invited Poster Presentations

1. U. Guin, M. Tehranipour, D. DiMase, and M. Megrđician, “**Counterfeit IC Detection and Challenges Ahead**,” ACM SIGDA, March 2013.
2. N. Reddy and M. Tehranipour, “**Reliability Analysis for 90nm Test Chips**,” Technical Reports, CADT-20110110, 2011.
3. F. Wu, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, M. Tehranipour, K. Miyase, X. Wen, N. Ahmed, “**Is Test Power Reduction Through X-Filling Good Enough?**,” Poster presentation, Int. Test Conference (ITC), 2010.
4. J. Lee and M. Tehranipour, “**Low-power Transition Delay Fault Test Pattern Generation**,” IEEE VLSI Test Symposium (VTS), 2008, PhD Thesis Poster Presentation.
5. M. Tehranipour, “**Trojan Detection and Isolation in Integrated Circuits**,” NSF Cyber Trust meeting, New Haven, March 2008
6. N. Ahmed, M. Tehranipour, and V. Jayaram, “**Considering IR-Drop Effects During Faster-than-at-Speed Delay Test**,” presented in Special Session (Elevator Talk), IEEE VLSI Test Symposium (VTS), 2006.
7. N. Ahmed and M. Tehranipour, “**On-chip Scan Enable Generation for Transition Fault Testing**,” Poster Presentation, University Booth, ITC 2005.
8. J. Plusquellic, D. Acharyya, C. Patel, A. Singh and M. Tehranipour, “**Hardware Investigation of Defect Sensitivity of a Multiple Supply Pad IDDQ Method**,” Poster Presentation, University Booth, ITC 2005.
9. N. Ahmed and M. Tehranipour, “**Enhanced Launch-off-Capture with Improved Fault Coverage and Reduced Pattern Count**,” Presented in UT-Austin Poster Session, ITC 2005.
10. M. H. Tehranipour and M. Nourani, “**Low-Power Test pattern generation for BIST Architecture**,” University of Texas at Dallas, 2003.

11. M. H. Tehranipour and M. Nourani, “**Test Compression and Power Reduction in Scan Using RL-Huffman Encoding.**” University of Texas at Dallas, 2002.

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1. **Consulting** with many companies (OCMs, OEMs, and EDA) and universities worldwide
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Invited Talks and Keynote Addresses

- **Keynote Speaker, Groundswell Conference on Cybersecurity**, Melbourne, FL, Nov. 2017
- **Invited Talk, Qualcomm**, San Diego, October 2017, Title: SoC Security
- **Invited Talk, Tsinghua University**, Beijing, October 2017, Title: *When it Comes to Security, Do not Forget about Hardware*
- **Keynote Speaker, Int. IEEE Verification and Security Workshop (IVSW)**, July 2017
- **Invited Talk: Air Force Research Laboratory (AFRL)**, Dayton, OH, Title: *Trusted and Assured Microelectronics*
- **Invited Talk: Air Force Research Laboratory (AFRL)**, Dayton, OH, Title: *Test and Design-for-Anti-Counterfeit*
- **Invited Talk: Ohio State University**, Columbus, OH, Title: *When It Comes to Cybersecurity, Do Not Forget About Hardware*
- **IEEE Ambassador talk at the Harris Corporation**, Melbourne, FL, March 2017, Title: *When It Comes to Cybersecurity, Do Not Forget About Hardware*
- **RSA Conference**, San Francisco, CA, February 2017, Title: *Securing Electronic Supply Chain from Design to Resign*
- **Keynote Speaker**, IEEE Asian HOST, Dec. 2016, Taiwan, Title: Security Rule Check
- **Keynote Speaker**, Microprocessor Test and Verification (MTV) Workshop, Austin, TX, Dec. 2016, Title: Security Rule Check: A Closer Look at the Automated Test for Security
- **Global Foundries, CTO Speaker Series**, Dec. 2016
- **Invited Talk: SRC e-Workshop**, July 2016
- **Invited Talk: Chinese Academy of Science (CAS)**, June 2016
- **Keynote Speaker:** International Workshop on on Hardware Security, 2016, Organized jointly by Tsinghua University and Beihang University, **Title:** Hardware Security: Past, Present, and the Future
- **Invited Talk: Peking University**, June 2016

- **Invited Talk: Beihang University**, June 2016
- **Invited Talk, Dagstuhl Seminar**, Germany, May 2016
- **Invited Talk: IEEE International Reliability Physics Symposium (IRPS)**, 2016, **Title:** *Security vs. Reliability: Where Do These Two Road Converge?*
- **Keynote Speaker: IEEE Workshop on CPS Security**, April 2016
- **Keynote Speaker: US-Brazil Joint Workshop on Cybersecurity**, April 2016, Orlando, FL
- **Invited Talk: Florida Institute of Technology (FIT)**, Host: Dr. Fareena Saqib, March 2016
- **Invited Talk: Florida Energy Systems Consortium (FESC)**, March 2016
- **Keynote Speaker: International Symposium on Quality Electronic Design (ISQED)**, Santa Clara, March 2016, **Title:** *New Frontiers in Hardware Security and Trust*
- **Invited Talk: Northrop Grumman**, Nov. 2015
- **Invited Talk: IEEE/ACM International Conference on Computer-Aided Design (ICCAD)**, Nov. 2015, Austin, TX
- **Invited Talk: Potomac Institute for Policy (PIP)**, October 2015
- **Invited Talk: DHS Software and Supply Chain Assurance Forum**, Sep. 2015
- **NSF WATCH Talk**, July 2015, Host: Jeremy Epstein
- **Invited Talk: Global Foundries**, Malta, NY, Dec. 2014
- **Keynote Speaker: Freescale Semiconductors' Technical Enrichment Conference**, Austin, TX, Dec. 2014
- **Invited Talk: Cadence**, Austin, TX, Dec. 2014
- **Invited Talk: Missile Defense Agency (MDA)**, Nov. 2014, Huntsville, Alabama
- **Invited Talk: Beihang University**, Nov. 2014, HOST: Prof. Michel Wang
- **Invited Talk: IEEE Asian Test Symposium (ATS)**, Nov. 2014
- **Invited Talk: Army Research Office (ARO) Workshop**, NYC, Nov. 2014
- **Invited Talk: CSI CyberSEED event**, University of Connecticut, Oct. 2014
- **Invited Talk: Honeywell International**, Oct. 2014
- **Invited Talk: ISE Northeast**, Oct. 2014, NYC
- **Invited Talk: Sharif University of Technology**, July 2014, HOST: Dr. Siavash Bayat
- **Invited Talk: Shahid Beheshti University**, July 2014, HOST: Dr. Ali Jahanian
- **Invited Talk: Amirkabir University of Technology**, June 2014, HOST: Drs. Saheb Zamani and Hamid Zarandi
- **Invited Talk: Cisco Corporation**, May 2014, Host: Dr. Wei Zhao
- **Invited Talk: Xilinx Corporation**, May 2014, Host: Dr. Amit Majumdar

- **Keynote Speaker: IEEE North Atlantic Test Workshop (NATW)**, May 2014
- **Invited Talk: Design, Automation, and Test in Europe (DATE)**, March 2014
- **Keynote Speaker: IEEE Int. Workshop on Reliability-Aware System Design and Test (RASDAT)**, Jan. 2014.
- **Invited Talk: IEEE Microprocessor Test Workshop**, Austin, TX, Dec. 2013
- **Invited Talk: DMSMS**, Dec. 2013, Counterfeit Detect Coverage
- **Invited Talk: DMSMS**, Dec. 2013, Combating Die/IC Recovery
- **Invited Talk: Missile Defense Agency (MDA), PMPB**, Nov. 2013
- **Invited Talk: ARO Workshop**, NYC, Nov. 2013
- **Invited Talk: Honeywell, Cyber Security Group Meeting**, Nov. 2013
- **Invited Talk: National Chao Tung University**, Taiwan, Nov. 2013
- **Invited Talk: MediaTek**, Taiwan, Nov. 2013
- **Invited Talk: CALCE Symposium on Counterfeit Electronic Parts and Electronic Supply Chain**, June 2013
- **Invited Talk: CS1 ICT Supply Chain Risk Management**, June 2013
- **Invited Talk: United Technologies Research Center (UTRC)**, May 2013
- **Invited Talk: NASA Quality Leadership Forum**, March 2013
- **Invited Talk: Trusted Supplier Industry**, March 2013
- **Invited Talk: Cisco, Security Group**, March, 2013, Title: SiliconAP: A novel Platform for Counterfeit Prevention
- **Invited Talk: ARO/CHASE Workshop on Counterfeit Electronics**, Jan. 2013, Counterfeit Detection Assessment
- **Invited Talk: ARO/CHASE Workshop on Counterfeit Electronics**, Jan. 2013, Silicon Authentication Platform
- **Invited Talk: NSF/SRC SA+TS Workshop**, Washington DC, Jan. 2013
- **Invited Talk: Microelectronics Reliability and Qualification proposal (MRQW)**, Dec. 2012
- **Invited Talk: DMSMS Standardization Conference**, Nov. 2012, Title: Secure Split Test for Counterfeit Avoidance
- **Invited Talk: DMSMS Standardization Conference**, Nov. 2012, Title: Counterfeit Test Technology Readiness Assessment
- **Invited Talk: IEEE Asian Test Symposium (ATS)**, Nov. 2012
- **Invited Talk: SRC e-Workshop**, Nov. 2012
- **Invited Talk: University of Arkansas**, Oct. 2012, HOST: Prof. Jia Di

- **Invited Talk: Symposium on Counterfeit Electronic Parts and Electronic Supply Chain**, June 2012
- **Invited Talk: University of Pittsburgh**, April 2012, HOST: Prof. Kartik Mohanram
- **Invited Talk: University of Illinois at Chicago**, March 2012, HOST: Prof. Wenjing Rao
- **Invited Talk: Missile Defense Agency**, March 2012, HOST: Fred Schipp
- **Invited Talk: San Jose State University**, March 2012, HOST: Prof. Shahab Ardalan
- **Invited Talk: G-19A Test Laboratory Standards Development Committee**, March 2012, HOST: Daniel DiMase, Honeywell
- **Invited Talk: IEEE International Reliability Innovations Conference (IRIC)**, March 2012 (Talk on Security)
- **Invited Talk: IEEE International Reliability Innovations Conference (IRIC)**, March 2012 (Talk on Reliability)
- **Invited Talk: IEEE Workshop on Defect and Adaptive Data Analysis (DATA)**, September 2011
- **Invited Talk: Air Force Research laboratory (AFRL)**, Rome, September 2011
- **Invited Talk: University of South Florida**, July 2011, HOST: Prof. Sanjukta Bhanja
- **Invited Talk: Low Power SOC Workshop (LPSOC)**, July 2011
- **Invited Talk: IBM TJ Watson**, June 2011, Host: Dr. Peilin Song
- **Invited Talk: Qualcomm**, June 2011, Host: Dr. Sagar Sabade
- **Invited Talk: Cisco**, May 2011, Host: Nemat Bidokhti and Bill Eklow
- **Invited Talk: IEEE VLSI Test Symposium (VTS)**, May 2011, Dana Point, CA
- **Invited Talk: Virginia Tech**, April 22, 2011, Host: Prof. Patrick Schaumont
- **Invited Talk: NYU-Abu Dhabi Workshop on Test**, New York, NY, April 2011, Host: Prof. Ozgur Sinanoglu
- **Invited Talk: University of Maryland**, April 2011, Host: Prof. Gang Qu
- **Invited Talk: ARO Workshop on Hardware Assurance**, Washington, DC, April 2010
- **Invited Talk: University of South Florida**, March 2011, IEEE CS Tampa Chapter, IEEE DVP program
- **Invited Talk: GOMACtech Conference**, March 2011, Orlando, FL
- **Invited Talk: LSI**, March 4, 2011, **Invited by: Sreejit Chakrabarty**, Title: On-chip Measurement Structures: Opportunities and Challenges
- **Invited Talk: LSI**, March 10, 2011, **Invited by: Arun Gunda**, Title: Detection of SDDs in Nanometer Technology Designs

- **Invited Talk: University of Wisconsin, Madison**, Feb. 2011
- **Invited Talk: MediaTek**, Boston, Nov. 2010. HOSTs: Jeff Roehr and Harry Chen
- **Invited Talk: Freescale**, Austin, TX, Nov. 2010, HOST: LeRoy Winemberg
- **Invited Talk: Texas Instruments**, Dallas, TX, September, 2010, HOST: Dr. Nisar Ahmed
- **Invited Talk: University of Texas at Arlington**, September 2010, Arlington, TX, HOST: Prof. Robert Magnusson, Title: Design for Hardware Security and Trust
- **Invited Talk: Air Force Research Lab (AFRL)**, Nov. 2011
- **Invited Talk: MediaTek**, Boston, Nov. 2010. HOSTs: Jeff Roher and Harry Chen
- **Invited Talk: Cisco**, October 2010, Hosts: Carson Stuart and Nemat Bidokhti, Title: New Threats to Hardware: Detection and Prevention Challenges
- **Invited Talk: Brown University**, Providence, RI, October 2010, Host: Prof. Sherief Reda, Title: Design for Hardware Security and Trust
- **Invited Talk: NYU-Poly**, New York, NY, August 2010, HOST: Prof. Ramesh Karri
- **Invited Talk: Qualcomm**, San Diego, CA, August 2010, HOST: Mike Laisne
- **Invited Talk: LSI**, June 2010, San Jose, CA, HOST: Dr. Sreejit Chakravarty
- **Invited Talk: Cisco**, June 2010, San Jose, CA, HOST: Nemat Bidokhti
- **Invited Talk: IBM**, May 2010, Invited by: Dr. Phil Nigh
- **Invited Talk: NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2010)**
- **Invited Talk: Connecticut Microelectronics and Optoelectronics Consortium (CMOC)**, 2010
- **Invited Talk: University of Massachusetts, Lowell**, March 2010, HOST: Prof. Martin Margala
- **Invited Talk: LSI Logic**, Jan 2010, HOST: Dr. Sreejit Chakravarty
- **Invited Talk: Information Security Council (INFOSEC)**, Jan 2010
- **Invited Talk: IBM-Austin Research Lab (IBM-ARL)**, Nov. 2009, HOST: Dr. Anne Gattiker
- **Invited Talk: ARO Special Workshop on Hardware Assurance**, 2009
- **Invited Talk: AMD**, July 2009, Host: Dr. Mahmut Yilmaz / Jeff Fitzgerald
- **Invited Talk: Amirkabir University of Technology**, July 2009, Host: Dr. A. Bagheri
- **Invited Talk: Cisco**, May 2009, Host: Nemat Bidokhti
- **Invited Talk: Southwest DFT (SWDFT-2009)**, Austin, TX
- **Invited Talk: Duke University**, April 2009, Host: Prof. Krishnendu Chakrabarty
- **Invited Talk: University of Rhode Island**, April 2009, Host: Prof. Resit Sendag
- **Invited Talk: Worcester Polytechnic Institute (WPI)**, March 2009, Host: Prof. Xinming Huang
- **Invited Talk: Mentor Graphics**, Feb 2009, Host: Dr. Yu Huang

- **Invited Talk: IBM TJ Watson**, Nov. 2008, Host: Dr. Jinjun Xiong
- **Invited Talk: Intel**, Nov. 2008, Title: *Small Delay Fault Detection and On-Chip Measurement*
- **Invited Talk: FIST**, Japan, Dec. 2008, Title: *Dealing with Power and Signal Integrity Issues During Test in Nanometer Technology Designs*
- **Invited Talk: University of Connecticut**, Title: *Hardware-Trust: Challenges and Solutions*
- **Invited Talk: IP/IC Trust, University of Connecticut, Northrop Grumman visit**
- **Invited Talk: Fukuoka Industry, Science & Technology Foundation (FIST)**, Japan, Dec. 2008, Title: *Verifying Trustworthiness of Integrated Circuits*
- **Invited Talk: Industry, Science & Technology Foundation (FIST)**, Japan, Dec. 2008, Title: *ATPG for Testing Power Supply Noise and Crosstalk*
- **Invited Talk: IEEE Workshop on Design for Reliability and Variability (DRV)**, Oct. 2008, Title: *ATPG for Increased Quality and In-Field Reliability*
- **Invited Talk: University of Tehran**, Host: Prof. Mahmoud Hashemi, Title: *ATPG for Increased Test Quality and In-field Reliability*
- **Invited Talk: University of Tehran**, Host: Prof. Mahmoud Hashemi, Title: *Verifying the Trustworthiness on Integrated Circuits*
- **Invited Talk: Sharif University of Technology**, Host: Prof. S. Ghassem Miremadi, Title: *ATPG for Increased Test Quality and In-field Reliability*
- **Invited Talk: Babol University of Technology**, Host: Prof. Miar Naimi, Title: *Verifying the Trustworthiness on Integrated Circuits*
- **Invited Talk: IBM**, Aug. 2008, Invited by: Dr. Phil Nigh
- **Invited Talk: Magma**, April 2008, Host: Dr. Sandeep Goel
- **Invited Talk: SRC e-Workshop**, Feb. 2008, Title: *High-Quality Delay Tests for Nanotechnology Designs*
- **Invited Talk: Freescale**, Austin, TX, Dec. 2007, Host: Dr. Magdy Abadir/Dr. Raj Raina
- **Invited Talk: Texas Instruments**, Dallas, TX, Dec. 2007, Hosts: Vinay Jayaram / Dr. Ken Butler
- **Invited Talk: TranSwitch**, Bedford, MA, Nov. 2007, Host: Zahi Abuhamdeh
- **Invited Talk: AMD**, Boston, MA, Nov. 2007, Host: Dr. Kamran Zarrineh
- **Invited Talk: Analog Devices**, Boston, MA, Nov. 2007, Host: Harry Chen
- **Keynote Speaker: Magma's Luncheon Event at International Test Conference (ITC)**, San Jose, CA, Tuesday Oct. 23, 2007

- **Invited Talk: Cadence**, June 2007, **Title:** *IR-drop Tolerant AT-speed Tests for Nanometer Technology Designs*, Host: Dr. Krishna Chakravadhanula
- **Invited Talk: LSI Logic**, June 2007, **Title:** *Generating High Quality At-speed Tests for Nanometer Technology Designs: Challenges and Solutions*, Invited by: Dr. Sreejit Chakravarty
- **Invited Talk: Qualcomm** (San Diego, CA), June 2007, **Title:** *At-speed Test for Nanotechnology: Challenges and Solutions*, Host: Dr. Sagar Sabade
- **Invited Talk:** Guest Lecturer for VLSI System Testing Course of ECE Department at **Duke University**, Instructor: Prof. Krish Chakrabarty
- **Invited Talk: Mentor Graphics** (Wilsonville, OR), Nov. 2006, **Title:** *At-speed Test for Nanotechnology: Challenges and Solutions*, Host: Dr. Nilanjan Mukherjee
- **Invited Talk: LSI Logic** (San Jose, CA), Nov. 2006, **Title:** *High Quality At-speed Tests for Nanotechnology Designs*, Host: Dr. Arun Gunda
- **Invited Talk: AMD** (Sunnyvale, CA), Oct. 2006, **Title:** *High Quality At-speed Tests for Nanometer High-speed Designs*, Host: Dr. Anuja Sehgal
- **Invited Talk: Texas Instruments** (Dallas, TX), April 2004, **Title:** Enhanced Scan Architectures for Reducing Power and Test Application Time

Technology Transfer

1. On-chip Monitors was successfully implemented on few products
2. Small-delay defect generation tool is used by semiconductor and EDA companies
3. LTG Cell for implementing LOS using low-speed scan enable signal
4. SAE International, the CDC tool on counterfeit detection
5. Test point insertion technology for LBIST to semiconductor industry

Teaching Experience

University of Florida

Spring 2018	EEL 4714/5716 Introduction to Hardware Security and Trust
Spring 2016	Introduction to Hardware Security and Trust

University of Connecticut

<u>Semester & Year</u>	<u>Course No. & Title</u>
Fall 2006	ECE 290: Senior Design
Spring 2007	ECE 291: Senior Design
Spring 2007	ECE 300: VLSI Design Verification and Test
Fall 2007	ECE 290: Senior Design

Spring 2008	ECE 291: Senior Design
Spring 2008	ECE 300: VLSI Design Verification and Test
Fall 2008	ECE 4901: Senior Design
Fall 2008	ECE 6094: VLSI CAD Algorithms
Spring 2009	ECE 3421: VLSI Design and Simulation
Fall 2010	ECE 6094: VLSI Design Verification and Test
Fall 2010	ECE 4901: Senior Design
Spring 2010	ECE 4095/6095: Intro. Hardware Security and Trust
Spring 2010	ECE 4902: Senior Design
Fall 2010	ECE 4095/6095: VLSI CAD Algorithms
Fall 2010	ECE 4901: Senior Design
Spring 2011	ECE 3421: VLSI Design and Simulation
Spring 2011	ECE 4902: Senior Design
Fall 2011	ECE 6432: VLSI Design Verification and Testing
Fall 2011	ECE 4901: Senior Design
Fall 2011	ECE 6094: Computer Engineering Seminar
Spring 2012	ECE 3401: Digital Systems Design
Spring 2012	ECE 4902: Senior Design
Spring 2012	ECE 6094: Computer Engineering Seminar
Fall 2012	ECE 4451/5451: Intro. to Hardware Security and Trust
Fall 2012	ECE 4901: Senior Design
Spring 2013	ECE 3401: Digital Systems Design
Spring 2013	ECE 4095: Hardware Hacking
Spring 2013	ECE 4902: Senior Design
Fall 2013	ECE 4901: Senior Design
Spring 2014	ECE 3401: Digital Systems Design
Spring 2014	ECE 4095: Hardware Hacking
Spring 2014	ECE 4902: Senior Design
Fall 2014	ECE 4451/5451: Intro. to Hardware Security and Trust
Fall 2014	ECE 4901: Senior Design
Spring 2015	ECE 4902: Senior Design
Spring 2016	EEL 4930: Introduction to Hardware Security and Trust

New Courses Developed and Taught at UMBC (2004-2006):

SOC Design and Test
CAD Algorithms
VLSI Design Verification and Testing

New Courses Developed and Taught at UConn:

VLSI Design Verification and Testing
CAD Algorithms
Introduction to Hardware Security and Trust
Hardware Hacking

New courses Developed at UF:

Introduction to Hardware Security and Trust

Research Group

Current Post-Doctoral Fellows and Visiting Researchers:

1. **Dr. Haoting Shen**, Post-doctoral Fellow (PhD, Penn State University), Jointly supervised with Prof. Domenic Forte
2. **Dr. Xiaolin Xu**, Post-doctoral Fellow (PhD, University of Massachusetts, Amherst), Jointly supervised with Prof. Domenic Forte
3. **Dr. Jungmin Park**, Post-doctoral Fellow (PhD, Iowa State University), Jointly supervised with Profs. Swarup Bhunia and Domenic Forte
4. **Dr. Qihang Shi**, Post-doctoral fellow (PhD, University of Connecticut), Jointly supervised with Prof. Domenic Forte

Current Graduate Students:

5. **Tony (Miao) He**, PhD Student, Spring 2013
6. **Fahim Rahman**, PhD Student, Fall 2013
7. **Adib Nahiyani**, PhD Student, Spring 2015
8. **Andrew Stern**, PhD students, Fall 2016
9. **Huanyu Wang**, PhD student, Fall 2016
10. **Mohammad Farmani**, PhD Student, Fall 2017
11. **Nidish Vashistha**, PhD Student, Fall 2017
12. **Jason Vosatka**, PhD Student, Fall 2017
13. **Nitin Pundir**, PhD Student, Spring 2018
14. **Sazadur Rahman**, PhD Student, Spring 2018

Current Undergraduate Students:

Former Students / Post-doctoral Fellows:

Post-doctoral fellow:

1. **Dr. Navid Asadi Zanjani**, 2014-2017, Currently with University of Florida
2. **Dr. Sina Shahbaz**, 2013-2014, Currently with University of Connecticut
3. **Dr. Shuo Wang**, 2010-2012, Currently with Qualcomm
4. **Dr. Hassan Salmani**, 2011-2013, Currently with Howard University

Graduate PhD Students:

1. **Nisar Ahmed**, PhD, Oct. 2007, Currently with Apple
2. **Junxia Ma**, Dec. 2010, Currently with Marvel
3. **Ke Peng**, Dec. 2010, Currently with ARM
4. **Xiaoxiao (Michel) Wang**, Dec. 2010, Currently with Beihang University as Full Professor as one of China's top 1000 talent
5. **Jeremy Lee**, Dec. 2010, Currently with Texas Instruments
6. **Hassan Salmani**, August 2011, Howard University
7. **Wei Zhao**, 2013, Currently with Nvidia
8. **Xuehui Zhang**, 2013, Currently with Oracle
9. **Jifeng Chen**, 2013, Currently with Samsung Research America
10. **Fang Bao**, 2014, Currently with Huawei
11. **Kan Xiao**, 2015, Currently with Intel
12. **Ujjwal Guin**, 2016, Currently an Assistant Professor at Auburn University
13. **Mehdi Sadi**, 2017, Currently with Intel
14. **Gustavo Contreras**, 2017
15. **Qihang Shi**, 2017, Currently a post-doc at the University of Florida
16. **Tauhidur Rahman**, 2017, Currently with the University of Alabama
17. **Kun Yang**, Jan 2018

Graduated M.Sc. Students:

1. **Halit Dogan**, Sep. 2013, Currently with University of Connecticut
2. **Niranjan Kayam**, M.S., Sep. 2011, Currently with Synopsys
3. **Prasath Periyasamy**, M.S. Thesis, Aug 2006, Currently with Qualcomm
4. **Smita Patil**, M.S. Project, Aug 2006, Currently with Atmel

5. **Mohammed ElShoukry**, M.S. Thesis, Aug 2006, Currently with Micron
6. **Eun Chung**, M.S. Project, Dec. 2004

Undergraduate Students:

1. Wesley Steven, 2014
2. Dan Guerrero, 2014
3. Ryan Nesbit, 2014
4. Shane Tobey, 2013
5. Shane Kelly, 2013-2014
6. Nathan Murphy, 2013
7. Jacquelyn Khajah, 2014
8. Andrew Ferraiuolo, REU-Sponsored Undergraduate Student, Summer & Fall 2011, Spring 2012
9. Ashley Calder, Undergraduate Student, Spring 2012
10. Michael Calvo, Eastern Conn. Univ., REU-Sponsored Undergraduate Student, Summer 2011
11. Sagar Patil, Undergraduate Researcher, Summer 2010
12. Ryan Fitterman (CMPE), Senior Design, 2012
13. Jeffrey Foster (EE), Senior Design, 2012
14. Alvin Sanabria (EE), Senior Design, 2012
15. Michael Stettenbenz (EE), Senior Design, 2012
16. Rifat Chowdhury (CMPE/MATH), Senior Design, 2012
17. Andrew Ferraiuolo (EE/CMPE), Senior Design, 2012
18. Adam Zimmer (CSE), Senior Design, 2012
19. Carl Hinkle (EE), Senior Design, 2011
20. Dan Matosian (CMPE), Senior Design, 2011
21. Ryan Wilson (EE), Senior Design, 2011
22. Emilio Cepeda (EE), Senior Design, 2011
23. Theodore Estwan (EE), Senior Design, 2011
24. Brian Helfer (EE), Senior Design, 2011
25. Sagar Patel (EE), Senior Design, 2010
26. Michael Runde (CMPE), Senior Design, 2010
27. Ton Thomas (CMPE), Senior Design, 2010
28. Nicholas Tuzzio (CMPE), Senior Design, 2010
29. Corey Benoit (EE), Senior Design, 2010

30. Joesph Larosa (EE), Senior Design, 2010
31. Kevin Perkins (EE), Senior Design, 2010
32. Andrew Tan (EE/MGMT), Senior Design, 2009
33. Colin Gladding (EE), Senior Design, 2009
34. Harpreet Mankoo (EE), Senior Design, 2009
35. Joe Mascola (EE), Senior Design, 2009
36. Elvis Anes (CMPE), Senior Design, 2009
37. Jeff Chua (CMPE), Senior Design, 2009
38. Ali Faraz (EE), Senior Design, 2009
39. Samantha Logue (CMPE), Senior Design, 2009
40. Poorak Mody (CMPE), Senior Design, 2008
41. Jonathan Schindler (CMPE), Senior Design, 2008
42. Jason Thibodeau (CMPE), Senior Design, 2008
43. Aaron Feldstein (EE), Senior Design, 2008
44. Paul Rago (EE), Senior Design, 2008
45. Danny Ho (EE), Senior Design, 2007
46. Kevin Tyler (EE), Senior Design, 2007
47. Vimal Vacchani (EE), Senior Design, 2007
48. Michael Kelley (EE), Senior Design, 2007
49. Benjamin Romeo (EE), Senior Design, 2007
50. Jeffrey Travis (EE), Senior Design, 2007
51. Pedro Almada, B.S., 2005

Thesis Advisory Committee

PhD Advisory Committee:

Nisar Ahmed (Chair), Jianwei Dai (Adivosr: Lei Wang, UConn), Wei-Gu Tang (Adivosr: Lei Wang, UConn), Janardhan Singaraju (Adivosr: John Chandy, UConn), Junxia Ma (Chair), Ke Peng (Chair), Michel Wang (Chair), Xuan Guan (Adivosr: Yunsi Fei), Jeremy Lee (Chair), Hai Lin, Shou Wang, Tina John (Adivosr: John Chandy, UConn), Abhishek Singh (Adivosr: Jim Plusquellic, UMB), Ajith Kumar (Adivosr: John Chandy, UConn), Robert Karam (Adivosr: Swarup Bhunia, UF), Fangchao Zhang (Advisor: Swarup Bhunia, UF), Zimu Guo (Advisor: Domenic Forte, UF), Kai Yang (Advisor: Swarup Bhunia, UF), Gustavo Contreras (Chair), Tauhid Rahman (Chair), Nima Karimian (Adivosr: Domenic Forte, UConn), Mahmut Yilmaz (Advisor: Krishnendu Chakrabarty, Duke University); Nolen Scaife (Advisor: Patrick Traynor, UF)

International: Fatemeh Ganji (Advisor: Jean-Pierre Seifert, TU Berlin), Shahin Tajik (Advisor: Jean-Pierre Seifert, TU Berlin)

M.S. Advisory Committee:

Halit Dogan (Chair), Niranjana Kayam (Chair), Prasath Periyasamy (Chair), Smita Patil (Chair), Mohammed ElShoukry (Chair), Eun Chung (Chair), Pushkar Pulastya, Michael Wolk, Jitin Tharian, Adhruva Acharyya, Niranjana Reddy, Shruti Khare, Michael Runda, Hitesh Sharma

B.Sc. Advisory Committee:

Jackson Carrol

Institutional Service

UF: ECE Department, Associate Chair for Research and Strategic Initiatives (2017-present)
UF: College of Engineering, Member, Research Advancement Committee, RAC (2017-present)
UF: ECE Department, Chair, Faculty Development Committee (2017-present)
UF: ECE Department, Member, Semotto IoT Chair Professorship Search Committee (2017-2018)
UF: College of Engineering, Tenure & Promotion (T&P) Committee (2017-2020)
UConn: Chair, Computer Engineering Search Committee (2012-2014)
UConn: ECE Search Committee (2011-2012, 2013-2014)
UConn: ECE Department Library Liaison, January 2009-Present
UConn: C&C Committee (2007-present)
UMBC: Member, Equipment Committee (Oct. 2004–2006)
UMBC: Member, Graduate Admission Committee (Jan 2005-2006)
UMBC: Member, ABET Visiting Committee (Oct. 2004–2006)

Supervising Undergraduate Senior Design Projects

2006-2007 **Project 1:** Redesign of Solitec Track System (Sponsored by Phonon)
 Project 2: Speech Control System for Persons with Disabilities (Sponsored by ECE Department) **First Prize in ECE Department**

2007-2008 **Project 1:** Wafer Processing Track Upgrade (Sponsored by Phonon) **Second Prize in ECE Department**
 Project 2: CAD2XML (Sponsored by QualTech)

2008-2009 **Project 1:** Digital Temperature Controller (DTC) Design (Sponsored by Phonon)
 Project 2: UConn Personal ATE (Sponsored by ECE Department)

2009-2010 **Project 1:** Surface Contour Profiler (Sponsored by Phonon) **First Prize in ECE Department**
 Project 2: UConn Personal ATE (Sponsored by ECE Department)

2010-2011 **Project 1:** Enhanced Surface Contour Profiler (Sponsored by Phonon) **First Prize in ECE Department**

Project 2: Distributed Aviation Control and Communication System (Sponsored by Hamilton Sundstrand)

2011-2012 **Project 1:** Automated Trojan Insertion and Detection Evaluation (Sponsored by ECE Department) **First Prize in ECE Department**

Project 2: Distributed Aviation Control and Communication System (Sponsored by Hamilton Sundstrand)

2013-2014 **Project 1:** Virtual Laboratir for Hardware Security (Sponsored by ECE Department)

2013-2014 **Project 2:** Automated Counterfeit IC Physical Defect Characterization (Sponsored by ECE Department)